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Technical Explanation SKiiP®4

Please note:
Unless otherwise specified, all values in this technical explanation are typical values. Typical values are the average values expected in large quantities and are provided for information purposes only. These values can and do vary in different applications. All operating parameters should be validated by user's technical experts for each application.

This document is valid for the following SKiiP®4 part numbers:

20601123	SKiiP 1814 GB12E4-3DUL
20601224	SKiiP 1814 GB17E4-3DUL
20601125	SKiiP 2414 GB12E4-4DUL
20601226	SKiiP 2414 GB17E4-4DUL
20601127	SKiiP 3614 GB12E4-6DUL
20601228	SKiiP 3614 GB17E4-6DUL
20601133	SKiiP 1814 GB12E4-3DUW
20601234	SKiiP 1814 GB17E4-3DUW
20601135	SKiiP 2414 GB12E4-4DUW
20601236	SKiiP 2414 GB17E4-4DUW
20601137	SKiiP 3614 GB12E4-6DUW
20601238	SKiiP 3614 GB17E4-6DUW
20601139	SKiiP 1814 GB12E4-3DUL
20601240	SKiiP 1814 GB17E4-3DUL
20601141	SKiiP 2414 GB12E4-4DUL
20601242	SKiiP 2414 GB17E4-4DUL
20601143	SKiiP 3614 GB12E4-6DUL
20601244	SKiiP 3614 GB17E4-6DUL
20601159	SKiiP 3614 GB12E4-6DULR
20601174	SKiiP 1814 GB12E4-3DUSL
20601175	SKiiP 2414 GB12E4-4DUSL
20601176	SKiiP 3614 GB12E4-6DUSL
20601277	SKiiP 3614 GB17E4-6DULR

as well as for the customized SKiiP®4 with part numbers 20601xxx (SKiiPxx-DUKxx) with restrictions according to the customer specification.The document remains effective until replaced by subsequent revision of this document.

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1 Related documents

- Data sheets SKiiP®4
- Diagnostic Interface SKiiP®4 – CANopen User Manual
- Diagnostic Interface SKiiP®4 – CANopen Object Dictionary
- Technical Explanation SKiiP®4 Parallel Board
- Technical Explanation SKiiP®4 F-Option
- Technical Explanation SKiFace Adapter Board

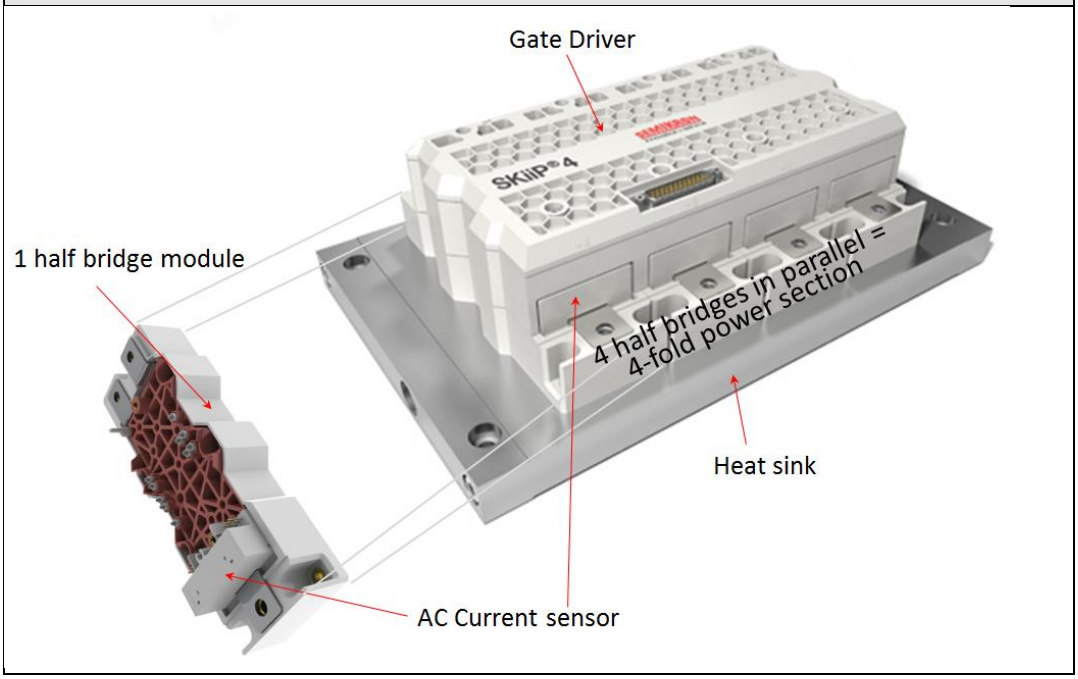
All these documents can be found on the SEMIKRON internet page.

2 Introduction

The 4th generation SKiiP, by name SKiiP®4, is an intelligent power module (IPM) with highest power density and reliability. SEMIKRON´s SKiiP stands for “SEMIKRON intelligent integrated Power” what means that three perfectly matched components are integrated to one IPM:

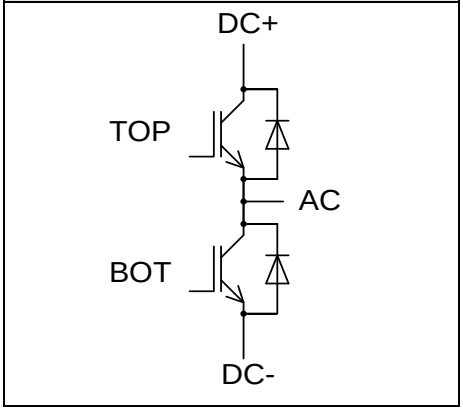
- heat sink
- power section
- gate driver

Figure 2.1: SKiiP®4 – 4 fold



The power section consists of 3, 4 or 6 in parallel connected half bridge modules whereas a half bridge is defined as shown in Figure 2.2. Explosion picture of half bridge module is shown in the Figure 2.3.The IGBT and the diode connected between DC+ and AC are named TOP IGBT / TOP diode. Consequently, the IGBT and the diode between AC and DC- are named BOT IGBT / BOT diode.

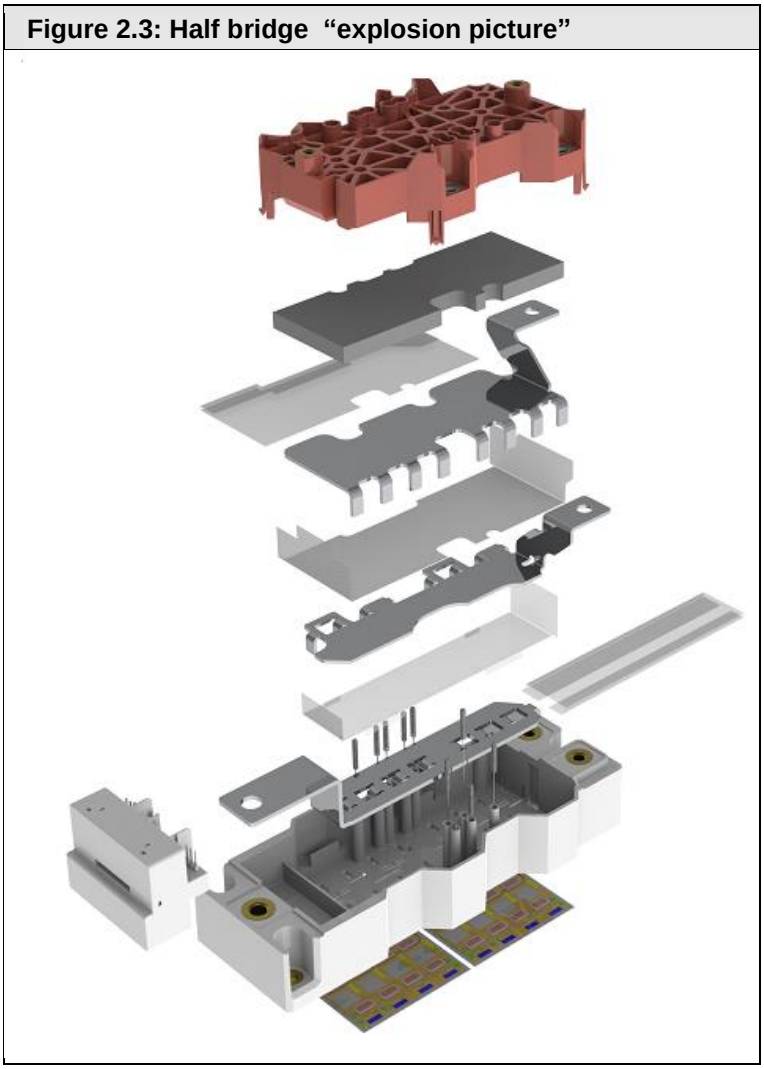
Figure 2.2: Half bridge definition



In this document following synonyms will be used for a power section with

- 3 half bridge modules in parallel = 3-fold
- 4 half bridge modules in parallel = 4-fold
- 6 half bridge modules in parallel = 6-fold

Figure 2.3: Half bridge "explosion picture"



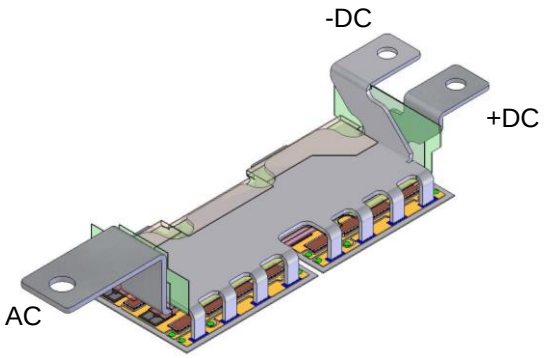
2.1 Heat sink

SEMIKRON offers high efficient water cooled heat sinks and air cooled aluminium heat sinks. Technical details are given in the corresponding datasheet. Customer specified heat sinks can be assembled on request as well. However there are several limitations, which should be strictly complied with to enable SEMIKRON to handle the customer specific heat sinks. Please refer to the PI 12-034 for additional information.

2.2 Power section

SKiiP®4 power section stays with its pressure contact technology without copper base plate. This means the Al_2O_3 DBC (direct bonded copper) substrate is pressed directly onto the heat sink without the use of a base plate. The pressure is induced by a pressure part on top, which is screwed to the heat sink. This pressure is transferred to the three main terminals (+DC, -DC and AC). These main terminals constitute a low-inductance sandwich construction and transfer the pressure to the above-mentioned DBC substrate. The pressure is applied across several contact points beside every single chip. As a result, a very low thermal and ohmic resistance $R_{CC'+EE'}$ is achieved (refer to Figure 2.4).

Figure 2.4: Main terminals construction principle



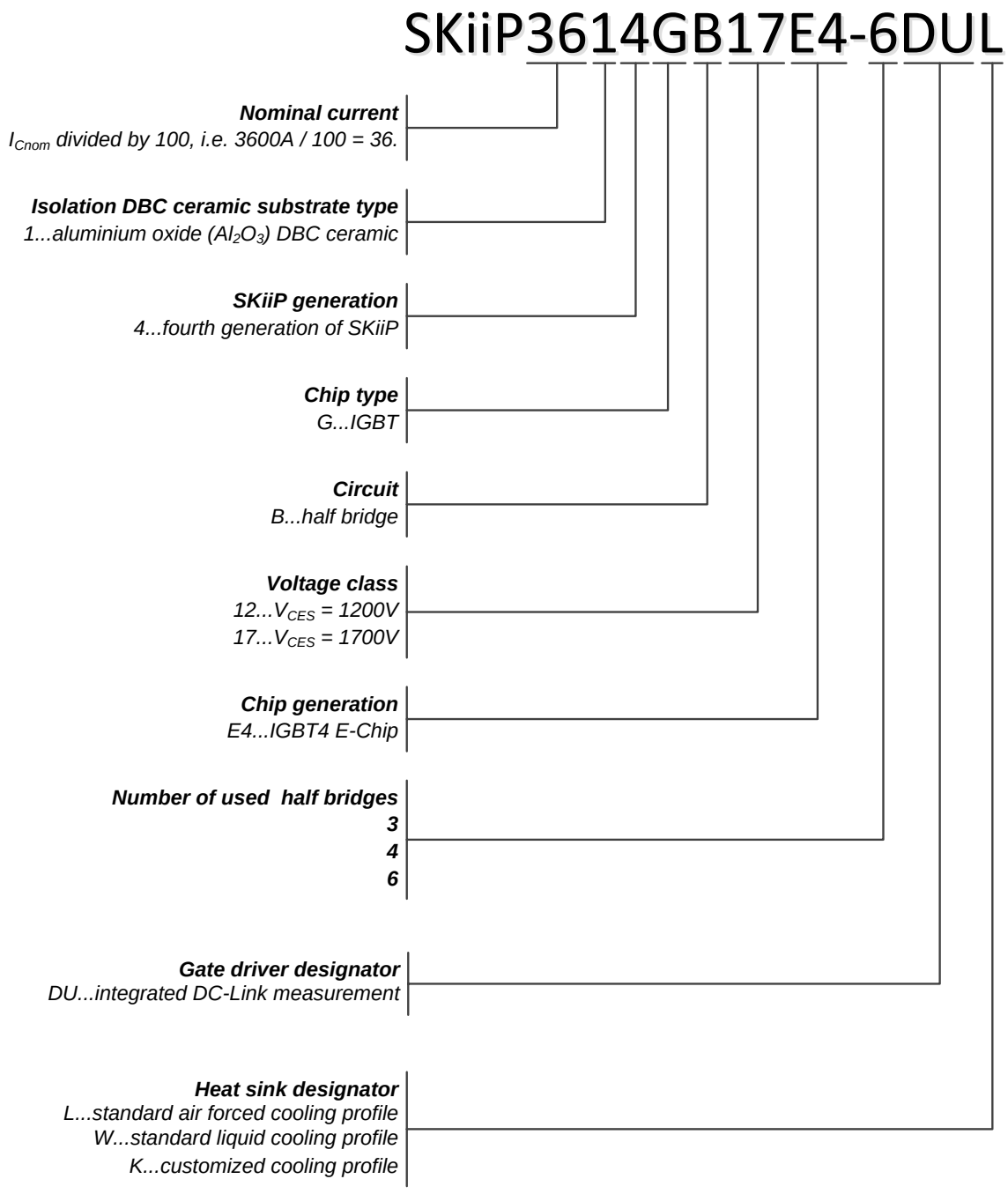
The chips themselves are sintered, not soldered. The sintering is based on pulverised silver which forms a material connection when pressure and temperature are applied.
Contact springs are used for all of the auxiliary contacts (gate, auxiliary emitter and temperature sensor). These spring contacts allow the solder-free connection of the driver board.

2.3 Gate Driver

The task of the driver unit is both transferring incoming signals into powerful output signals to control the IGBT and to ensure signal isolation between high and low voltage sides of the driver board. Additionally, fault conditions need to be monitored to protect the power section in case of a failure. For an effective failure analysis a serial diagnostic I/O based on the CAN open protocol was implemented.

3 Topologies and selection guide

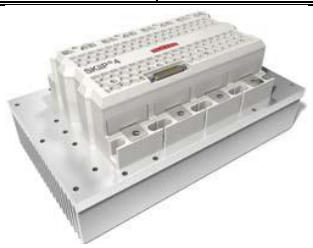
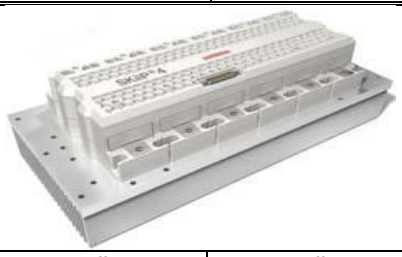
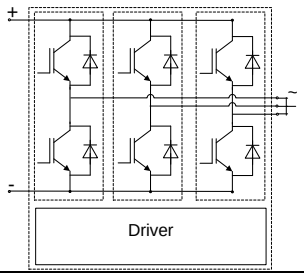
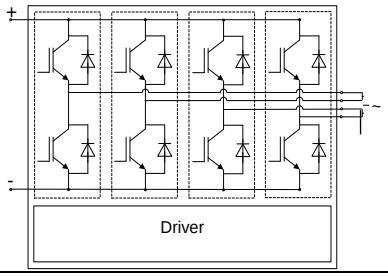
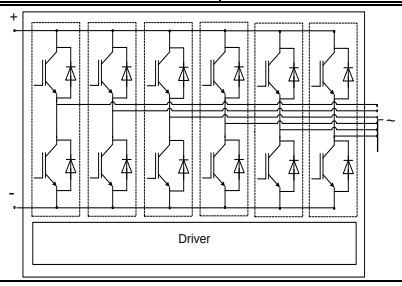
3.1 Type Designation Code



3.2 Overview of the available types and current ratings

The Table 3-1**Fehler! Verweisquelle konnte nicht gefunden werden.** gives an overview of the available types and current ratings (I_{Cnom}).

Table 3-1: SKiiP®4 standard product range

3-fold		4-fold		6-fold	
					
SKiiP 1814GB12E4-3DUW	SKiiP 1814GB17E4-3DUW	SKiiP 2414GB12E4-4DUW	SKiiP 2414GB17E4-4DUW	SKiiP 3614GB12E4-6DUW	SKiiP 3614GB17E4-6DUW
					
SKiiP 1814GB12E4-3DUL	SKiiP 1814GB17E4-3DUL	SKiiP 2414GB12E4-4DUL	SKiiP 2414GB17E4-4DUL	SKiiP 3614GB12E4-6DUL	SKiiP 3614GB17E4-6DUL
					
I_{Cnom} = 1800A		I_{Cnom} = 2400A		I_{Cnom} = 3600A	

4 Standards and qualification tests

4.1 Tests for qualification and re-qualification

Table 4-1: SKiiP®4 Tests for qualification and re-qualification

No	Test	Test Conditions	Standard
01	High Temperature Reverse Bias	1000h, V_{GE} = 0V, 95% V_{CEmax} T_s=T_{jmax}-10°C	IEC 60747-9
02	High Temperature Gate Stress	1000h, +/- V_{GEmax}, T_{jmax}	IEC 60747-9
03	High Humidity High Temperature Reverse Bias	1000h, 85°C, 85% RH, $V_{CE\ max.}$=1360 V, V_{GE}=0V	IEC 60068 Part 2-67
04	High Temperature Storage	1000h, T_a = +125°C	IEC 60068 Part 2-2
05	Low Temperature Storage	1000h, T_a = -40°C	IEC 60068 Part 2-1
06	Thermal Cycling	100 cycles, -40°C/ +125°C	IEC 60068 Part 2-14
07	Power Cycling (EOL-Test)	60.000 load cycles @ ΔT_j = 110K, T_{jm}=95°C 200.000 load cycles @ ΔT_j = 70K, T_{jm}=115°C	IEC 60747-9
08	Vibration (Halt Test)	Sinusoidal Sweep, 5g, x, y, z – axis, 2h/ axis	IEC 60068 Part 2-6
09	Shock (Halt Test)	Halfsinusoidal Pulse, 30g, +/- x, +/- y, +/- z direction, 1000 times per direction	IEC 60068 Part 2-27
10	Corrosive gas test	Ta = 25°C, 75%RH, 4 components: H_2S (hydrosulfide), NO_2 (nitrogen dioxid), Cl_2 (Chlor), SO_2 (Sulphur dioxid), 21 days	IEC 60068 Part 2-60

4.2 Electromagnetic compatibility (EMC)

The SKiiP®4 is designed to withstand the following immunity tests with EMC compliant installation:

Table 4-2: SKiiP®4 Electromagnetic compatibility

Immunity test	Conditions	Test level
Fast transients (Burst) (61000-4-4)	On driver board interfaces	4kV / 5kHz
Radio Frequency Fields (61000-4-3)	Polarisation: vertical + horizontal Frequency: 80 MHz - 1000 MHz Modulation: 80% AM, 1kHz Far field, homogeneous Stripline acc.11425-5 level III/F3	 20V/m 200V/m
RF Conducted Disturbance (61000-4-6)	Frequency: 150 kHz - 80 MHz Modulation: 80 % AM, 1kHz	Voltage: 20V EMF
Magnet field (61000-4-8)	Far field, homogeneous	170A/m
Electrostatic discharge (ESD) EN 61000-4-2	Contact discharge Air discharge	6kV 8kV

4.3 Isolation coordination

The isolation of the SKiiP®4 is designed according to EN50178 and EN61800-5-1. For working conditions please refer to the datasheet SKiiP®4.

Table 4-3: Isolation limits SKiiP®4	
Isolation / Test level	**Min value**
Creepage primary - secondary	14mm
Creepage secondary – heat sink potential	8mm
Clearance primary – secondary	14mm
Clearance secondary – heat sink potential	8mm
Partial discharge extinction voltage (IEC60664-1) between primary and secondary side of driver board	1900V rms; Q_{PD} < 10pC
Rated impulse voltage (IEC60664-1) primary to secondary and primary to heat sink	8kV 1,2/50µs

4.4 Installation altitude

Isolation coordination for SKiiP®4 is done for overvoltage category III and altitudes up to 2000m.
The required clearance distances between mains-circuits and their environment for overvoltage category III are listed in EN50178.
For an earthed-neutral system the rated isolation voltage is defined in chapter 5.2.16.1 of EN50178 as:
"…the peak value of the rated voltage between phase and earthed neutral point."
Based on this sentence the rated isolation voltage in case of a grounded delta grid (Figure 4.1) and a star grounded grid (Figure 4.2) can be derived as:
Rated isolation voltage in case of 690V grounded delta grid: 690V
Rated isolation voltage in case of 690V star grounded grid: 400V

Figure 4.1: Grounded delta grid

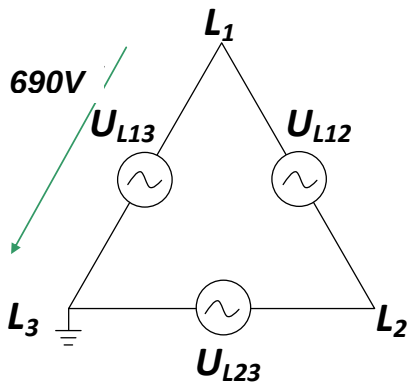
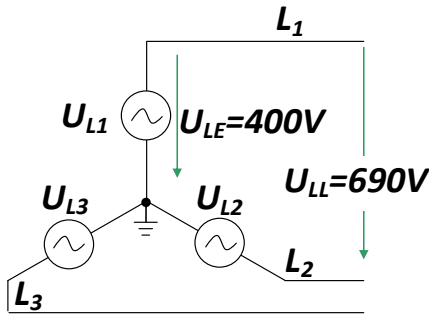


Figure 4.2: Star grounded circuit network (690V-TN-grid)



Based on the kind of grid and the voltage level the required clearance distances for basic and reinforced isolation differ from the designed ones.
According to HD625 S1 and IEC60664-1 the maximum altitude can be calculated based on the factors between required and designed clearance distances.

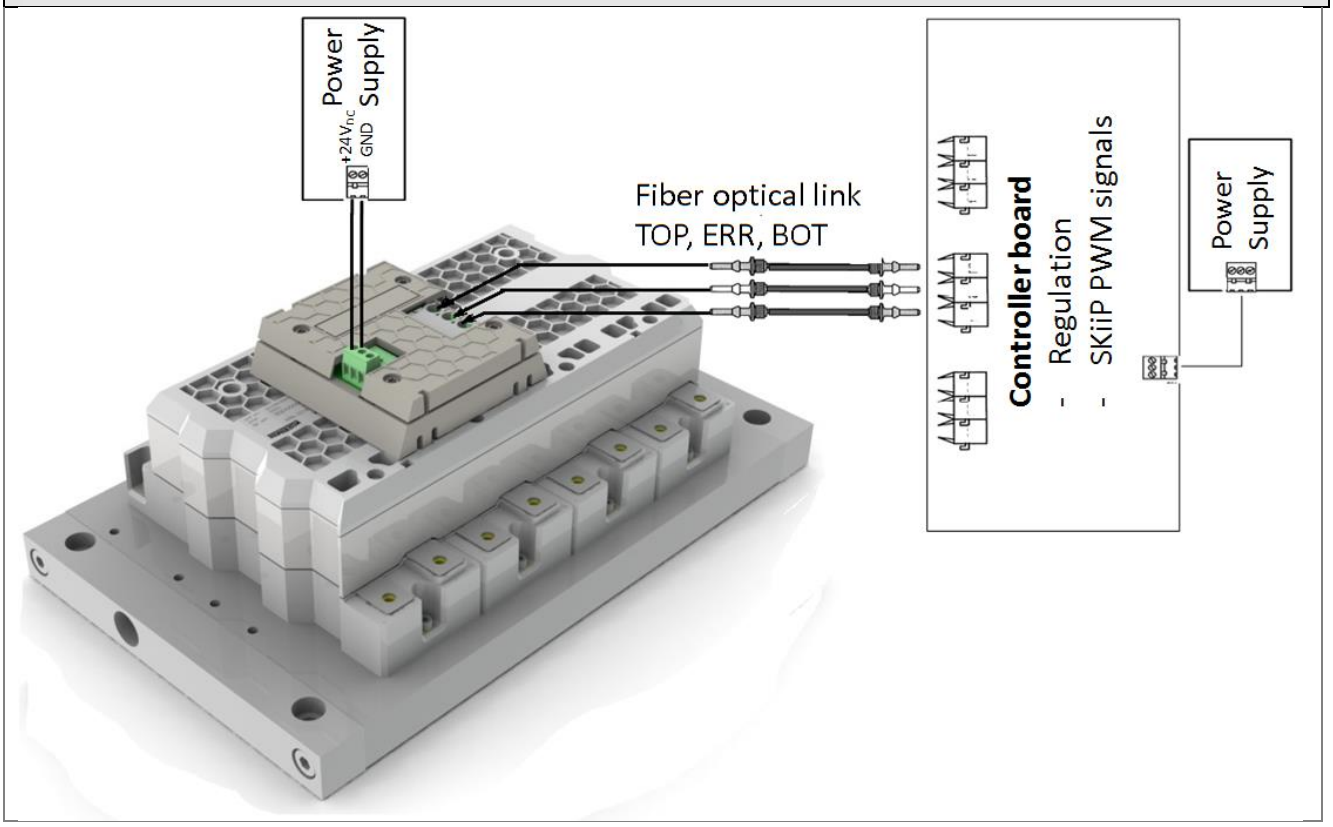
Table 4-4: Altitude correction factors (IEC 60664-1)		
Altitude	Normal barometric pressure	Multiplication factor for clearances
m	kPa	
2 000	80,0	1,00
3 000	70,0	1,14
4 000	62,0	1,29
5 000	54,0	1,48
6 000	47,0	1,70
7 000	41,0	1,95
8 000	35,5	2,25
9 000	30,5	2,62
10 000	26,5	3,02
15 000	12,0	6,67
20 000	5,5	14,5

The overvoltage category influences the installation altitude too. To increase the altitude further the overvoltage category need to be reduced (EN50178):
"As an alternative to the values of table 3, columns 2 to 5, the clearances between mains-circuits of an EE and its environment may be designed in accordance with overvoltage category II, if facilities are provided which reduce overvoltages of category III to values of category II…However for reinforced isolation according to column 7 shall ***not*** *be reduced."*
The required clearance distances between mains-circuits and their environment for overvoltage category II are listed in EN50178.
If safety isolation is necessary the maximum altitude of SKiiP®4 is 6250 m (690 TN grid and overvoltage category II).
If only basic isolation is required even higher altitudes are possible. In case of 690V TN grid and overvoltage category II an altitude of theoretically 9000 m for SKiiP®4 is possible.
This is the case when an additional basic isolation is implemented between SKiiP driver interface and controller board. This can be realized by the following means:

- Use of fiber optic for control signals (TOP, BOT, Error) and
- SKiiP analogue signals (current, DC-voltage and temperature measurement) are not used and
- all SKiiPs are supplied by separate power supplies on which no other circuit is connected.

The above described implementation is shown in the Figure 4.3. The F-Option board for SKiiP®4 (it is shown in the Figure 4.3) can be ordered separately and can be easily mounted on the SKiiP4 top cover.

Figure 4.3: Implementation of additional basic isolation between SKiiP®4 driver interface and controller board

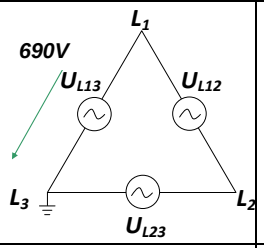
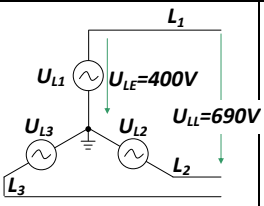
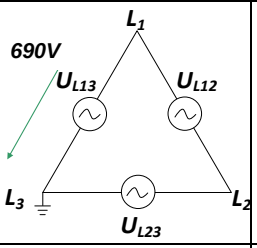
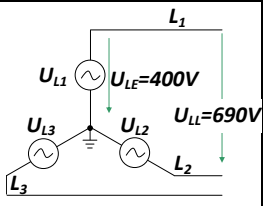


Finally, the installation altitude of SKiiP depends on:

- The kind of grid (star grounded grid, delta grounded grid)
- The voltage level of the line to earth voltage (rated isolation voltage)
- The overvoltage category (II or III)
- Whether safety isolation is required or not

Table 4-5 summarizes the installation altitudes for SKiiP®4.

Table 4-5: Installation altitudes for SKiiP®4 in dependency of kind of grid, overvoltage category and kind of required isolation

SKiiP4 (with 690V grounded delta)		Overvoltage category III		Overvoltage category II	
		Grounded delta grid	TN 690V	Grounded delta grid	TN 690V
					
Basic isolation against ground	Required for 2000m	8 mm	5,5 mm	5,5 mm	3 mm
	Existing	8 mm			
	Factor	1	1,45	1,45	2,66
	Altitude	**2000m**	**4840m**	**4840m**	**9000m**
Reinforced isolation	Required for 2000m	14 mm	8 mm	14mm	8mm
	Existing	14 mm			
	Factor	1	1,75	1	1,75
	Altitude	**2000m**	**6250m**	**2000m**	**6250m**
Maximum Altitude with safety isolation		**2000m**	**4840m**	**2000m**	**6250m**
Maximum Altitude without safety isolation		**2000m**	**4840m**	**4840m**	**9000m**

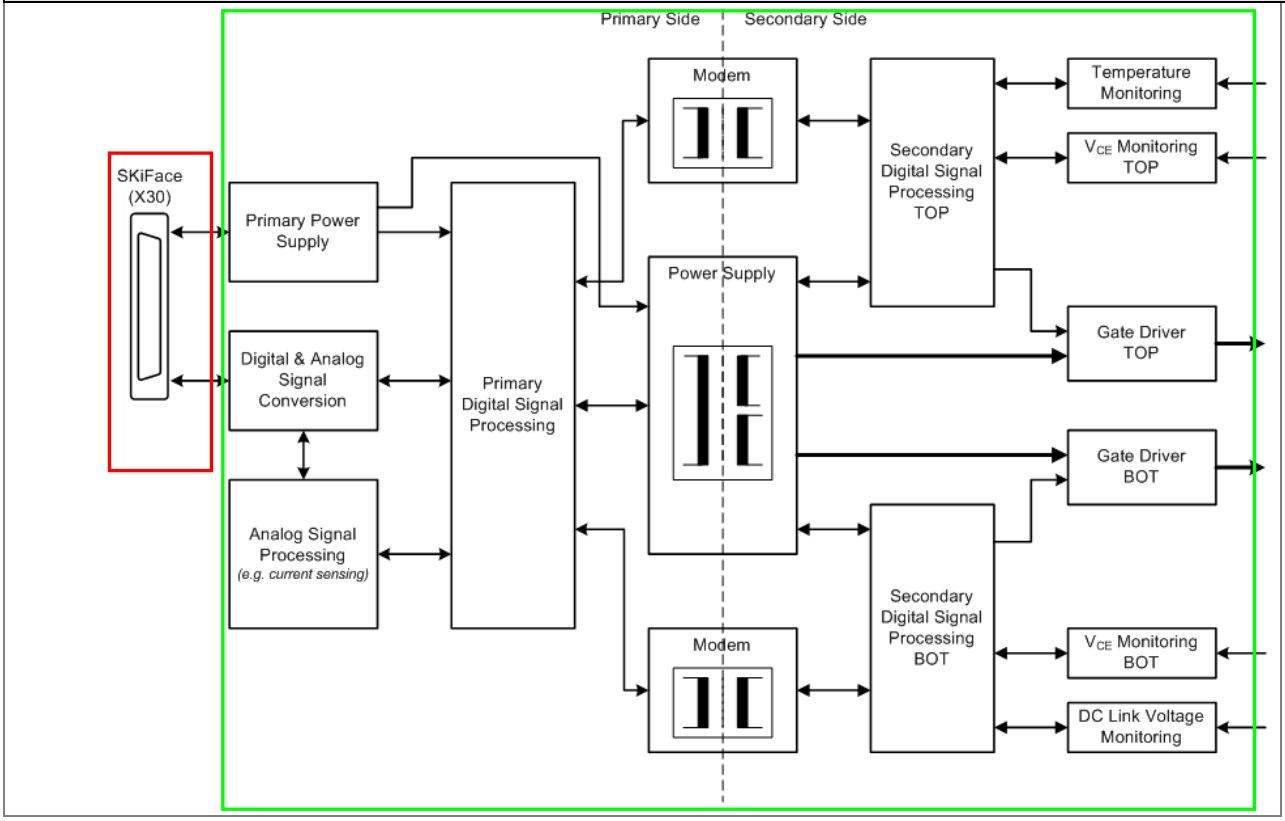
5 Gate Driver Board

5.1 Overview

The functionality of the Gate Driver can be seen in following block diagram.

- Gate driver interface SKiFace, red block in the Figure 5.1 (refer to Chapter 5.2)
- Gate driver board, green block in the Figure 5.1 (refer to Chapter 5.3)

Figure 5.1: Gate Driver Board block diagram



5.2 Gate driver interface “SKiFace”

5.2.1 Overview

The Gate Driver Interface SKiFace is marked in Figure 5.2. It is a 25 pin D-Sub male plug connector. The picture, the pin-out and the dimensions are summarized in Figure 5.3.
It includes Pins for:

- External Power Supply (refer to chapter 5.2.3)
- Switching signal input (refer to chapter 5.2.4)
- Analogue signals (refer to chapter 5.2.5)
- HALT logic (refer to chapter 5.2.6)
- CMN_GPIO output (refer to chapter 5.2.7
- CAN interface (refer to chapter 5.2.8)

Figure 5.2: Gate Driver Interface

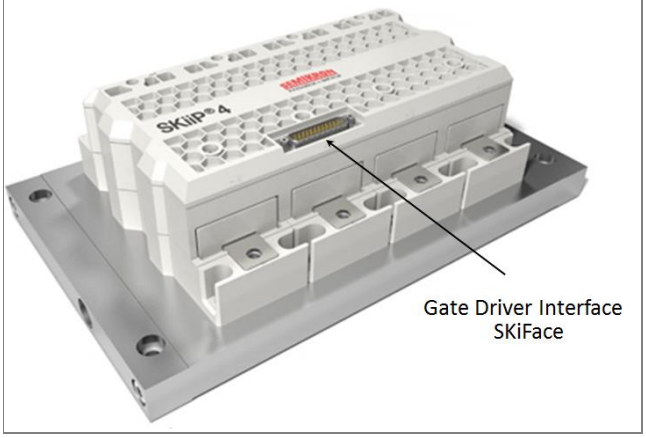
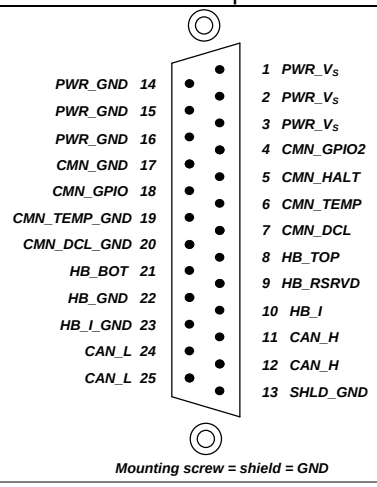
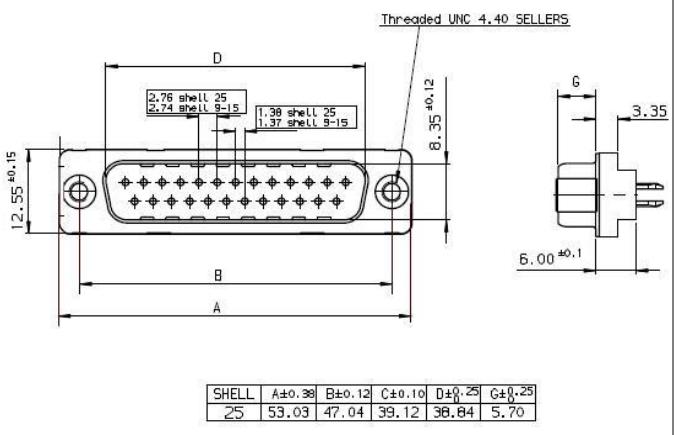


Figure 5.3: SKiiP®4 - connector D-Sub 25 pin, male plug, vertical, top view

Picture	Pin Description	Dimensions





For connecting the SKiiP®4 to a controller the following recommendations should be considered when choosing a cable:

- Cable length should be kept shorter than 3m
- Usage of shielded cables is recommended
- Longer cables must be shielded

Verification according to mechanical stability and EMC behaviour in customer’s application is necessary.

As the SKiFace interface is a standard one it is also used for other SEMIKRON products. Due to that not all signals are used for SKiiP®4.
Not used signals are: CMN_GPIO2, HB_RSRVD

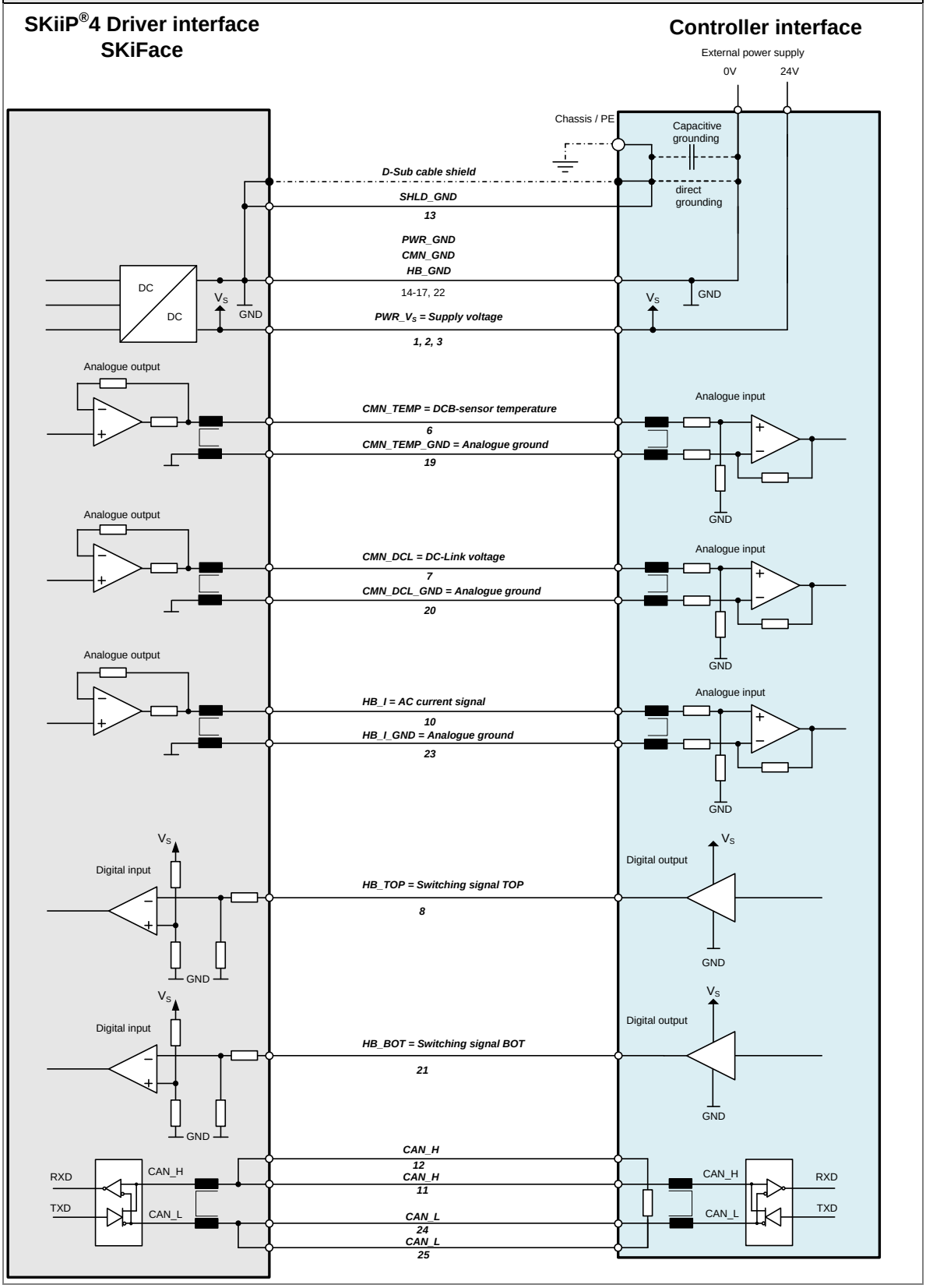
Please note: The plastic cover of D-Sub connector should be removed shortly before the start of operation (ESD-Handling)

5.2.2 Pin description

Table 5-1: Pin description SKiiP®4

PIN	Signal	Function	Specification
1/2/3	PWR_V_S	Power Supply	+24V (+/- 20%)
4	CMN_GPIO2	Reserved	Not used
5	CMN_HALT	Digital input/ output Bidirectional status signal	LOW (dominant) = not ready to operate (e.g. error) HIGH (recessive) = ready to operate For details see HALT Logic Signal, p. 24
6	CMN_TEMP	Temperature signal out	This pin is used to transmit the differential temperature sensor analogue signal. Max output current: 5mA Nominal voltage range: 0 … +10V See Integrated DCB-Temperature Sensor, p.40
7	CMN_DCL	DC-Link voltage out	This pin is used to transmit the differential DC-Link voltage level. Max. output current: 5mA Nominal voltage range: 0 … +10V For details see DC-Link-Voltage Sensing,p.41
8	HB_TOP	Switching signal input for high side IGBT	LOW = High side IGBT off HIGH = High side IGBT on For details see Switching Signal Inputs, p.21
9	HB_RSRVD	Reserved	Not connected
10	HB_I	Current sensor out	This pin is used to transmit the differential current sensor analogue signal. Max. output current: 5mA Nominal voltage range: -10V … +10V For details see AC-current sensor, p.37
11	CAN_H	CAN interface INPUT/ OUTPUT HIGH	Input impedance = infinite Specification according to ISO 11898.
12	CAN_H		Internally connected to pin 11
13	SHLD_GND	GND	Internally connected to PWR_GND
14/15/16	PWR_GND	Ground for PWR_V_S	
17	CMN_GND	Ground for CMN_HALT, CMN_GPIO	Internally connected to PWR_GND
18	CMN_GPIO	Digital Input/Output General purpose IO	Inverted CMN_HALT signal (exept in case of activated FRT-function, please refer to chapter CMN_GPIO signal, p. 26
19	CMN_TEMP_GND	Ground for CMN_TEMP	
20	CMN_DCL_GND	Ground for CMN_DCL	
21	HB_BOT	Switching signal input for low side IGBT	LOW = Low side IGBT off HIGH = Low side IGBT on For details see Switching Signal Inputs, p.21
22	HB_GND	Ground for CMN_HB_TOP, CMN_HB_BOT, CMN_HB_RSRVD	Internally connected to PWR_GND
23	HB_I_GND	Ground for HB_I	
24	CAN_L	CAN interface INPUT/ OUTPUT LOW	Input impedance = infinite; Specification according to ISO 11898.
25	CAN_L		Internally connected to pin 24

Figure 5.4: Overview schematics SKiFace interface (CMN_GPIO and CMN_HALT are not depicted)



The left side shows the equivalent circuit diagram of the driver board with ground connections. The right side shows an application example for the controller side.

5.2.3 External Power Supply

Table 5-2 shows the required features of an appropriate external power supply for a SKiiP®4.

Table 5-2: Requirements to the auxiliary power supply	
Power supply	The maximum ratings for the supply voltage are given in the SKiiP®4 data sheet on page 1 (refer to symbol V_s). The supply voltage is defined at the SKiiP®4 input, not at the controller output (voltage drop on connection cable)
Maximum rise time of 24V	<2 s
Rated current	1,5 times of the maximum driver input current
Minimum peak current	2 times of the maximum driver input current (At least 1,5A)

Please note: Do not apply switching signals during power up.

The external power supply may not be turned-off for a short time as consequence of its current limitation. Its output characteristic needs to be considered. Power supplies with fold-back characteristic or hiccup-mode can create problems if insufficient over current margin is available. The voltage has to rise continuously and without any plateau formation.
In order to ensure continuous operation and to have some margin in case of overload it is recommended to choose the rated current of the external power supply higher than the maximum driver input current (see symbol I_s on page 2 of the corresponding SKiiP®4 datasheet).
If the power supply is able to provide a higher current, a peak current will flow in the first instant to charge up the input capacitances on the driver. The peak current value will be limited only by the external power supply and the effective impedances (e.g. distribution lines). It is recommended to avoid the paralleling of several customer side external power supply units. Their different current limitations may lead to drops in the supply voltage.
The formula given in the SKiiP®4 datasheet for calculating the supply current I_S (page 2) consists of three parts:
The first part is the current consumption of the driver during Standby. No switching signals are applied. Consequently, no AC-current flows. Example below is given for SKiiP2414GB17E4 (I_{SO}=360mA).
The second part is the required current consumption of the driver during switching.
The third part is the current consumption required by the integrated current sensor to compensate the present value of the AC-current.

$$360mA + k_1 \cdot f_{sw} + k_2 \cdot I_{AC}$$

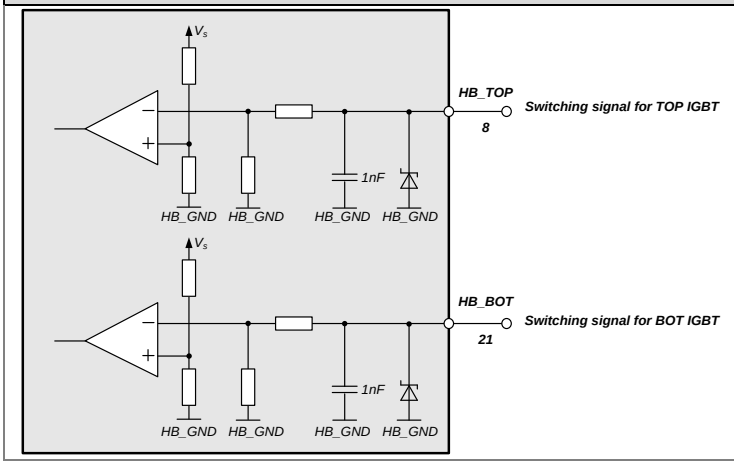
- $k_2 \cdot I_{AC}$: Current consumption of integrated current sensor
- $k_1 \cdot f_{sw}$: Current consumption of driver during switching
- $360mA$: Standby current consumption of the driver

5.2.4 Switching Signal Inputs

The switching signal inputs HB_TOP for the TOP and HB_BOT for the BOT IGBT have a digital positive / active high logic (input HIGH = IGBT on; input LOW = IGBT off) characteristic.
For driving the inputs HB_TOP and HB_BOT it is mandatory to use line drivers with a push-pull charactersitic. Pull up and open collector output stages must not be used for driving these inputs. It is recommended to choose the line drivers (e.g. IXDD604) according to the demanded length of the signal wires.

Please note: A non connected input will be considered as LOW signal.

Figure 5.5: TOP/BOT PWM Signal Input



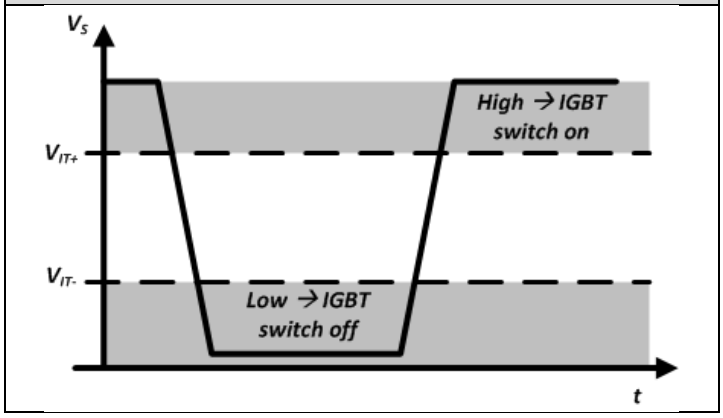
A 1nF capacitor is connected to the switching signal input to obtain high noise immunity. This capacitor can cause a delay of few ns for current limited line drivers, which can be neglected.

Input resistance is about 13kOhm

As shown in Figure 5.7. the switching signal will be considered as:

- High when > V_{IT+}
- Low when < V_{IT-}

Figure 5.6: Threshold level for HB_TOP and HB_BOT



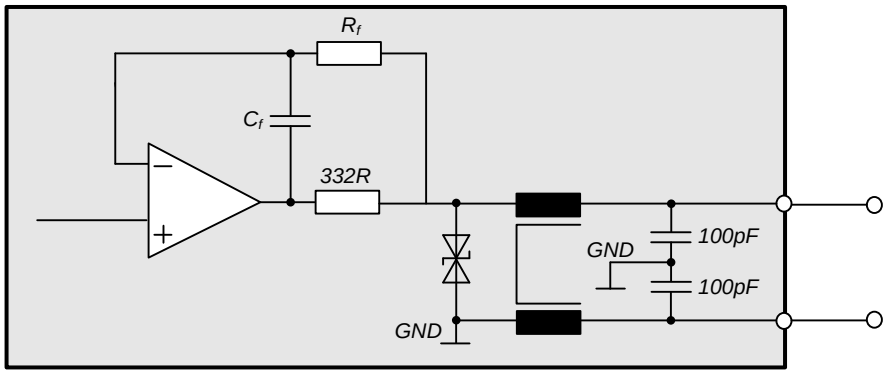
The threshold values V_{IT+} and V_{IT-} are given in the SKiiP®4 datasheet on page 2.
For V_{IT+} the value is given as minimum value that is *at least* necessary in order to switch on the IGBT.
For V_{IT-} the value is given as maximum value that should not be exceeded in order to switch off the IGBT.
All threshold values are related to the supply voltage V_s.

5.2.5 Analogue Output Signals

The schematic in the Figure 5.7 shows the analogue output circuit of the gate driver.
This circuit is part of:

- Measurement of AC-current
- Measurement of DC-link voltage
- Measurement of DCB-sensor temperature

Figure 5.7: Schematics analogue output signals



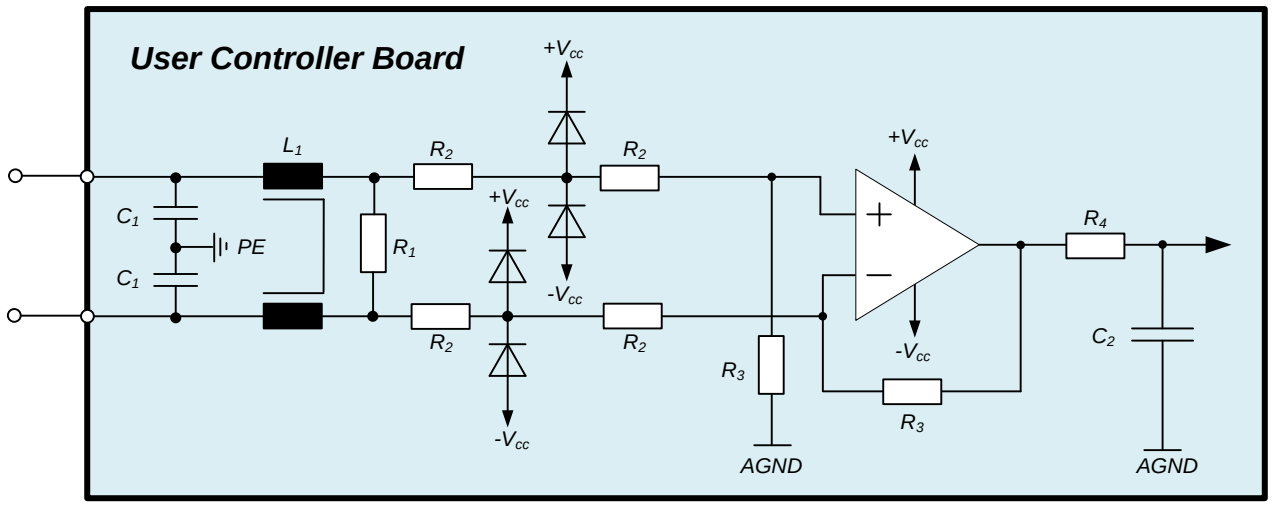
The 332Ω resistor avoids damages caused by a temporary short circuit at the analogue output.

Please ensure that the maximum driven current by the output operational amplifier does not exceed 5mA.

A common mode choke and 100pF capacitors are used on the outputs to obtain high noise immunity.
On the user controller board a differential amplifier should be used which is connected to the analogue output and the corresponding ground signals (CMN_TEMP_GND, CMN_DCL_GND, HB_I_GND). This ensures accurate measurement of the analogue signals because there is no voltage drop on the analogue ground wires due to the high input impedance of the differential amplifier (refer to Figure 5.13).

A description for an equivalent analogue input circuit on the user controller board is given in Figure 5.8.

Figure 5.8: Application Example – Symmetric Wired differential Amplifier. Terminal description HB_I and HB_I_GND for current measurement



The recommended values below have to be checked in the application.

- The equivalent input capacitance should not be higher than 1nF for current measurement and 10nF for temperature and voltage measurement to achieve stable operation of the amplifier circuit on the SKiiP®4 board. Its signal response has to be checked in combination with the used signal cable.
- C1 leaks differential and common mode high-frequency interference currents. This capacitor reduces the bandwidth of the analogue signal. This can lead to regulation problems like AC current harmonics. Depending on application PE should be connected to an appropriate ground, e.g. chassis ground.
- Common Mode Choke L1 is used for filtering of common mode currents. The current-compensated ring core choke with ferrite core and rating 51µH/0,5A is recommended.
- Resistor (R1). The interference sensitivity of the overall circuit (user control, driver) is reduced by a continuous current flow through this resistor. Recommended value: 10kOhm

Please note: Capacitors should not be used in parallel to the feedback resistor (R3) and also to the resistor of the non-inverting input to ground (R3). These capacitors have often high tolerances, so the common-mode rejection of the circuitry is reduced by this effect. There should be no capacitor between the plus- and the minus-pin of the operational amplifier as well. This additional corner frequency can lead to an oscillating signal.

- The input resistor (R2) should be splitted up and installed between the clamping-diodes. The current in the diodes is limited by this resistor. A diode with a low reverse current should be selected e.g. BAV99.
- To achieve a good noise performance a low-impedant feedback-resistor should be used (R3). Recommended value: 25kOhm.
- A low pass filtering should be implemented to avoid remaining differential interferences. It can be realised by a simple R-C network (R4, C4) at the end of operational amplifier. The corner frequency of the filter should be adjusted with the behaviour of the operational amplifier used and the necessary bandwidth of the analogue signal (Temp/DC-Link/Current).
- If not using Rail-to-Rail amplifier, it is recommended to connect the pin $-V_{CC}$ to negative voltage instead of ground in order to use the complete voltage range of the amplifier, especially close to 0V. The possible negative output voltage of the amplifier has to be considered for designing the following circuit.
- AGND should be connected to the ground of the analogue signal processing at the user controller board.

5.2.6 HALT Logic Signal

Characteristics and functionality:

- enables and disables the Gate driver
- dominant/recessive (settable and readable by driver and user controller board)
- low active (LOW = IGBT driver disabled, HIGH = IGBT driver enabled)
- digital signal referred to the driver supply voltage V_S

The driver will set the HALT signal to LOW state during power on reset, if a write-access via CAN takes place and if the error is present (refer to chapter 5.3.7).
The driver will automatically set the HALT signal to HIGH state:

  - after power-on reset time has elapsed ***and*** if no error is present
  - after error reset time has elapsed ***and*** if no error is present ***and*** both signal inputs TOP and BOT are LOW
  - after CAN write-access is completed

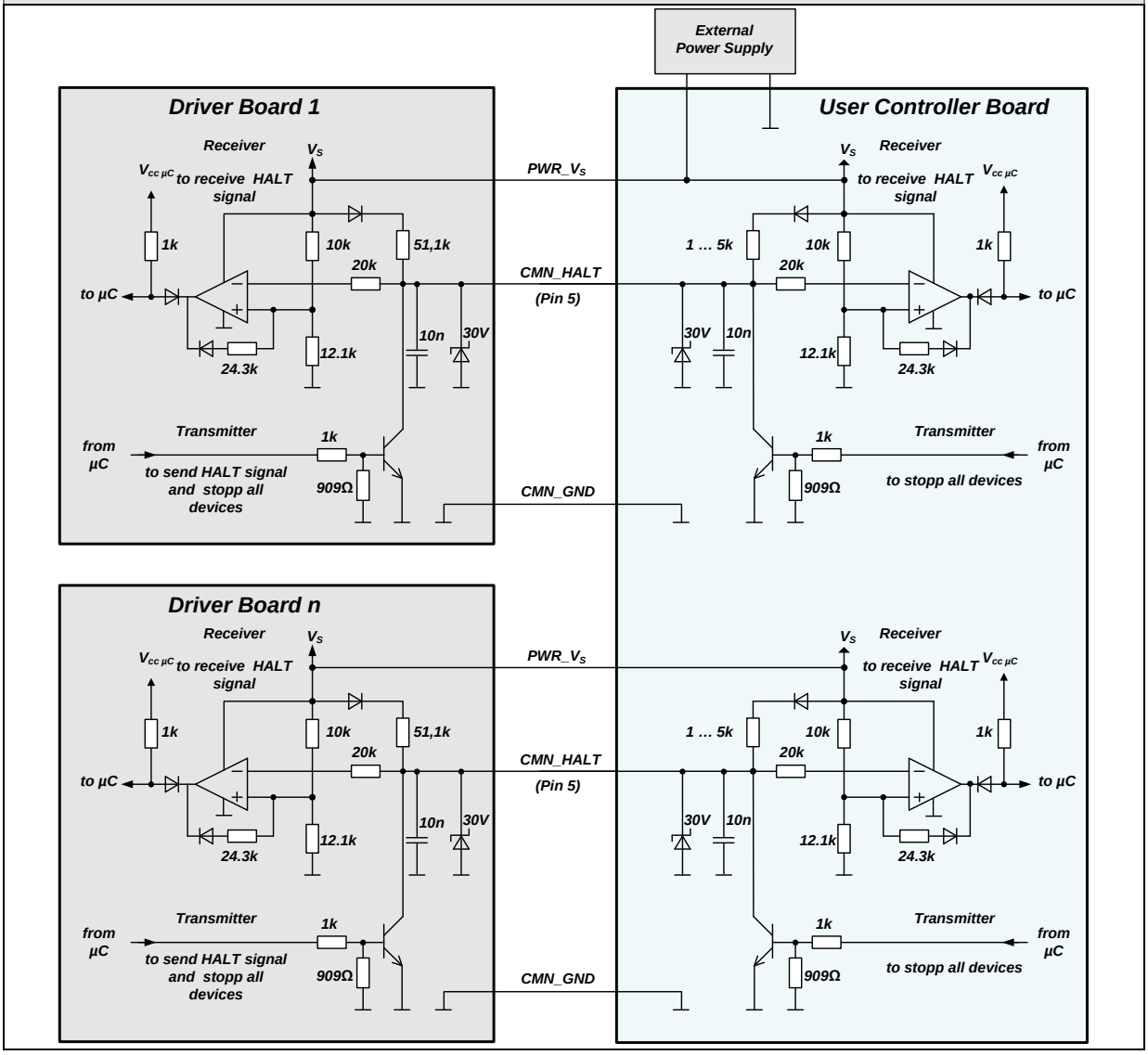
The HALT signals of all SKiiPs in the application and also from other hardware components can be connected together. That means that the HALT signal is set to LOW state when one of the connected SKiiPs is not ready to operate.

Please note: There is no possibility to see which SKiiP®4 set the HALT signal. For this purpose the CAN-diagnostic interface should be used

This parallel connection of HALT signals offersa fast disabling of IGBT switching in case of an error or power up of paralleled components. Operation can only be started when all components are ready to operate. This is an useful function during start-up.The HALT signals of all SKiiPs in the application could also be connected to the controller separately as shown in the Figure 5.9. The circuit on the driver board is shown on the left hand side. The Gate Driver can be set into HALT state by pulling the CMN_HALT signal to GND at the user controller board.

The HALT signal is pulled to GND by a transistor. Pull up resistors are connected on each driver board and on the user controller board. In order to keep the current low when several SKiiP units are connected in parallel the pull up resistor on the driver board is relatively high (51,1kOhm). The pull up resistor on the user controller board should be at least 1kOhm. The delay of the HALT signal due to the capacitors on driver board (10nF) must be considered.

Figure 5.9: Application example of the HALT signal for separate connected SKiiP®4 systems



Please note: If HALT signal is not used it must be connected to the V_s according to the Figure 5.16 (not used digital signals).

5.2.7 CMN_GPIO signal

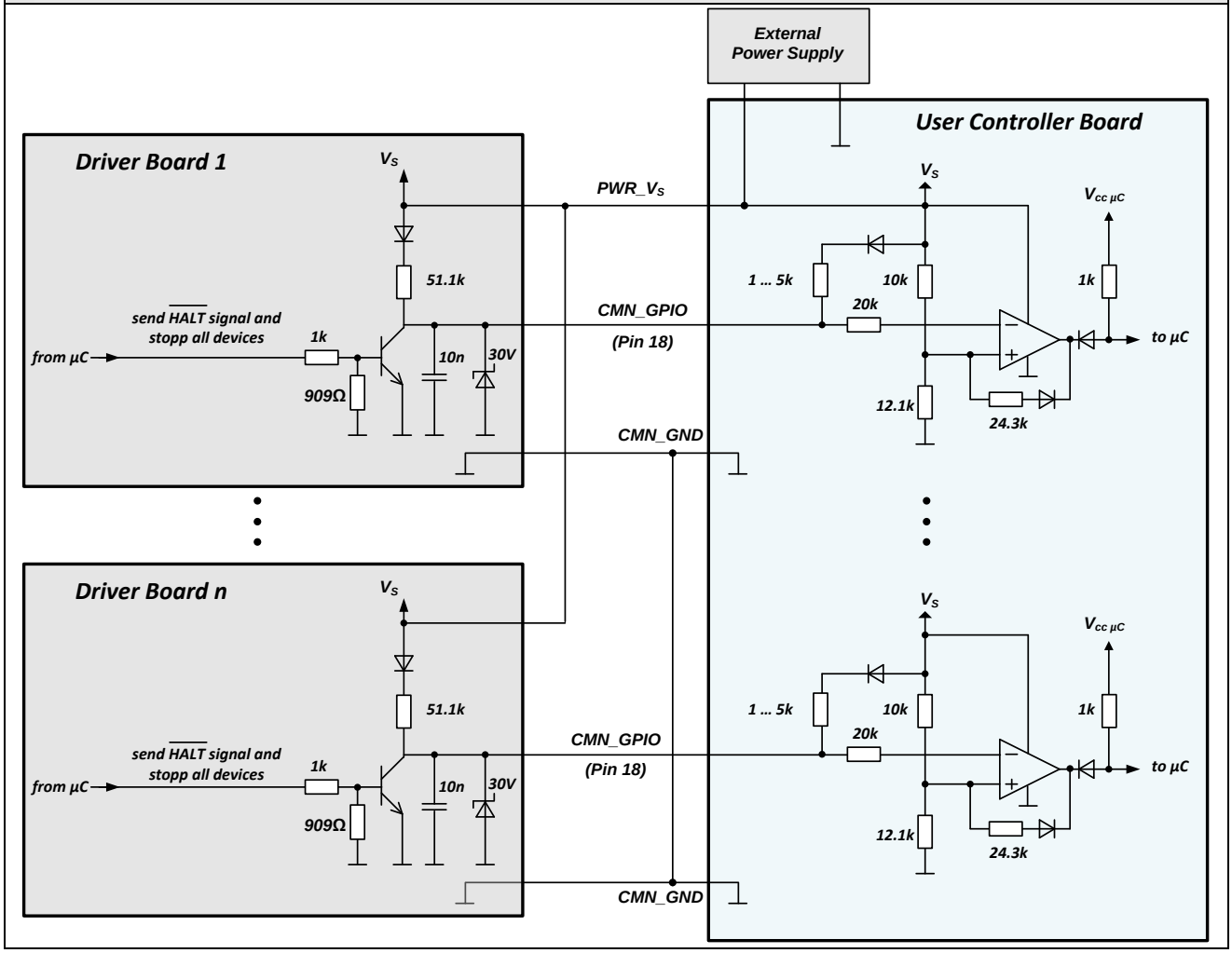
The CMN_GPIO signal is available at Pin 18 of SKiFace interface.
The CMN_GPIO signal is the inverted HALT signal ($\overline{HALT}$) that can be used as error output signal of the SKiiP®4 (in case of activated FRT-function please refer to chapter 7.7 for further information).

Please note: As far as CMN_GPIO signal is the inverted HALT signal there is no possibility to see which SKiiP4 has sent the error output signal. For this purpose the CAN-diagnostic interface should be used

Figure 5.10 depicts:

- on the left hand side the output stage of the CMN_GPIO signal
- on the right hand side an example of the input stage on the user controller board for each CMN_GPIO output of several SKiiP®4

Figure 5.10: Application example of the CMN_GPIO (inverted HALT signal) as error output signal



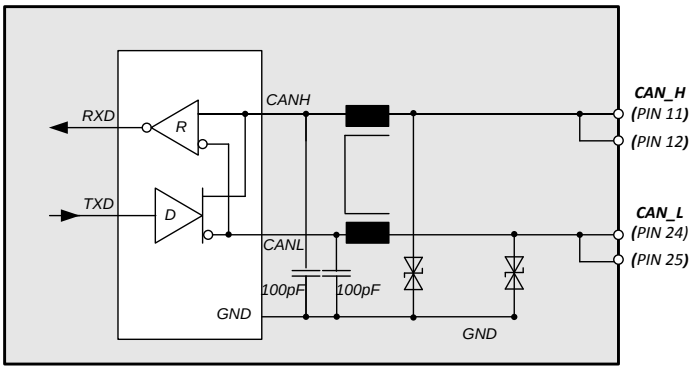
5.2.8 CAN-Interface

The CAN-Interface offers the possibility to read out exact error time, kind and source of the error. In addition to this the CAN-interface can be used for activation/deactivation some optional features of SKiiP®4 as for example FRT-function (see Chapter 7.7) or DC-Link Trip level deactivation.

> Please note: By deactivation of V_{DCtrip} the max value ratings from the corresponding SKiiP4 data sheet must be strictly observed. The violation of these limits can lead to the threat to life or physical condition, as well as to the damage of SKiiP.

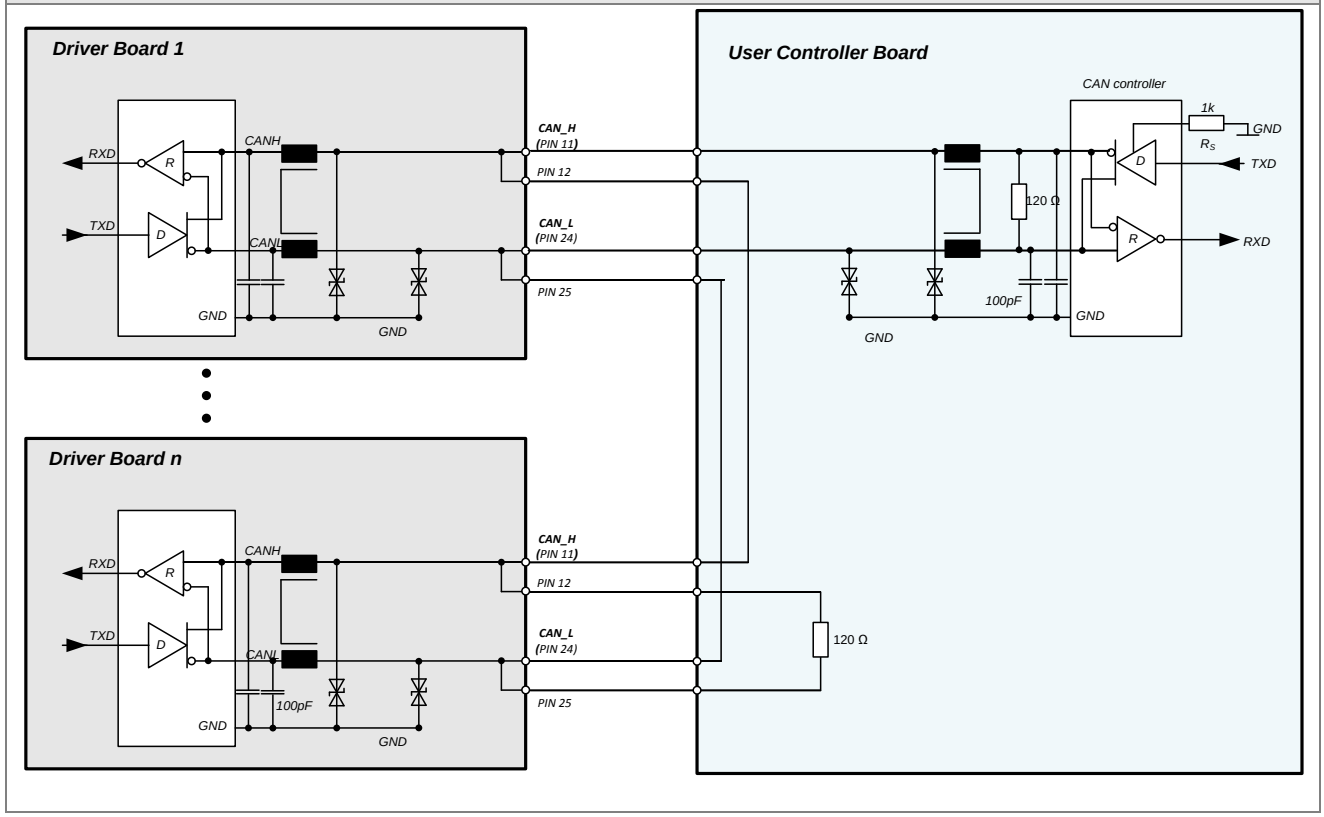
The CAN-Interface is available at the Pins 11 and 12 (CAN_H) and at the Pins 24 and 25 (CAN_L) as shown in Figure 5.11.

Figure 5.11: CAN-Interface



If several SKiiP®4 are used the CAN – application example as shown in Figure 5.12 is recommended.

Figure 5.12: CAN – application example for several SKiiP



For a detailed description of the SKiiP4 CAN interface please refer to the documents

- Diagnostic Interface SKiiP4 – CANopen User Manual
- Diagnostic Interface SKiiP4 – CANopen Object Dictionary

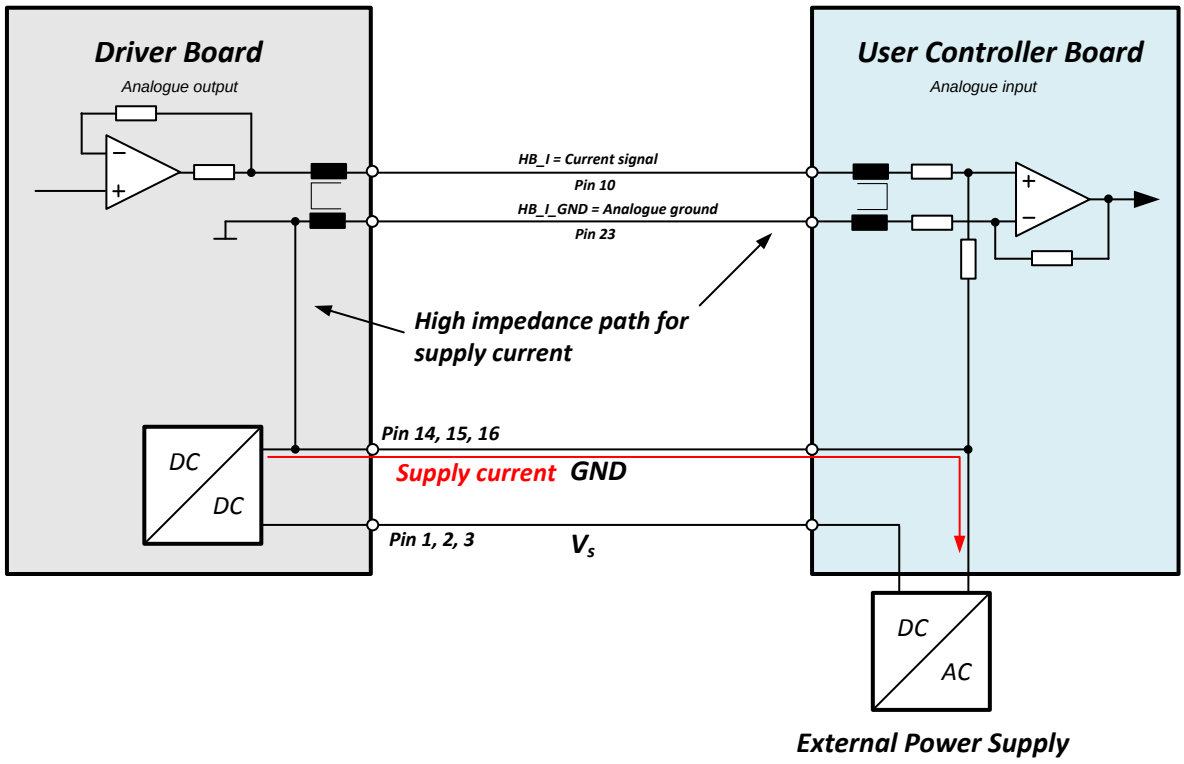
5.2.9 Ground connection

SKiiP®4 has power grounds, digital grounds and analogue grounds. The power ground and digital grounds are used for power supply and reference of digital signals, respectively. The analogue ground is used for accurate measuring of analogue signals. All grounds are physically connected to each other on the Gate Driver board. It is allowed to short-circuit all ground potentials in exception of the analogue grounds on the user controller board.
These analogue grounds should be used for differential amplifier input on the controller board to ensure accurate measurement (refer to Figure 5.13). The availability of several power and digital ground connections makes it possible to use additional components in the ground connection on controller side for higher noise immunity like common mode chokes if it is needed.

Table 5-3: Ground connections of SKiiP®4

Function	Signal
Power ground and digital grounds	PWR_GND CMN_GND HB_GND
Analogue ground	CMN_TEMP_GND CMN_DCL_GND HB_I_GND

Figure 5.13: Prevention of ground loops due to differential amplifier



5.2.10 Shield and protective earth/chassis connection

The shield of the D-Sub connector is connected to GND at the Gate Driver board. There is no connection at the Gate Driver board to heat sink nor other protective earth connections. On the user controller board the shield should be connected to chassis which is protective earth in isolation class 1 systems. This single ended grounding is effective against capacitive coupling e.g. from neighbouring conductors since the grounded shield forms the opposite pole of the parasitic capacitance. The interference current flows away via the shield. The GND of the user controller board can be connected to protective earth/chassis either directly or via a capacitor. This connection should be low inductive (e.g. metal bolts from PCB to chassis) and located close to the D-Sub connector. Further each signal output and input should have a capacitor to chassis. These measures are for bypassing burst signals.

Figure 5.14: Ground and shield connection. Principle schematics for Ground and shield connection. Principle schematics for switching signal inputs

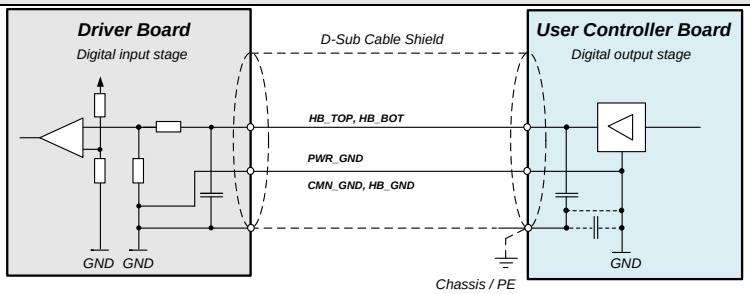
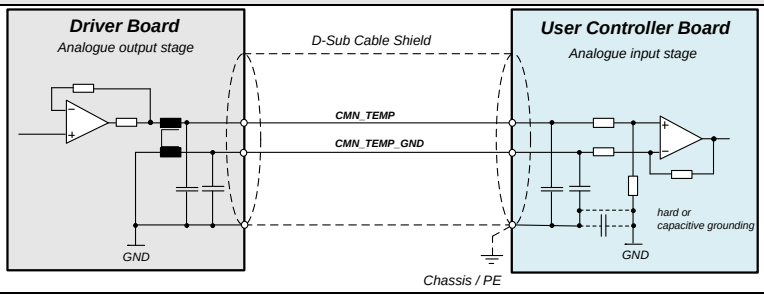


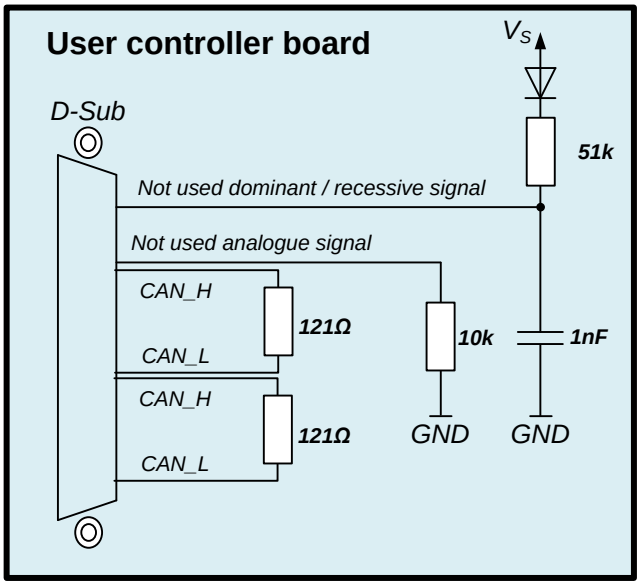
Figure 5.15: Ground and shield connection. Principle schematics for analogue output signal (Example: Temperature output)



5.2.11 Reserved or not used signals

Not used pins for digital signals (CMN_GPIO2, CMN_GPIO) at the user controller board should be connected to V_S by 51kOhm resistor in series to a diode as shown in Figure 5.16.
The diode prevents supplying of the controller by the driver board when the controller is not supplied. Also a capacitor should be connected to GND to shorten burst signals.
For the CAN interface it is recommended to short the CAN open signals by 121 Ohm resistor, if the CAN interface will not be used.
Not used analogue signals should be connected to GND by a 10kOhm resistor.

Figure 5.16: Connection of reserved and not used signals at the user controller board



5.3 Gate driver board

5.3.1 Overview

The SKiiP®4 gate driver board includes following functions:

- Digital signal transmission (refer to chapter 5.3.2)
- Power-on Reset (refer to chapter 5.3.3)
- Dead time generation (refer to chapter 5.3.4)
- Short pulse suppression (refer to chapter 5.3.5)
- IntelliOff switching (refer to chapter 5.3.6)
- Failure management (refer to chapter 5.3.7)

This driver is based on digital signal processing which provides individual control parameter settings and the transmission of galvanic insulated sensor signals. The digital signal processing ensures a high level of signal integrity and hence high noise rejection. Overvoltages, especially those that occur in short-circuit turn-off conditions, are reduced by the Gate Driver by means of intelligent turn-off control.
The gate voltages are +15V for turn on and -8V for turn off.

5.3.2 Digital signal transmission

The driver board has two independent signal channels from low voltage to high voltage sides for transferring of switching and sensor signals. The signals are transferred by pulse transformers which are designed for reinforced isolation. The signals are differential signals.This ensures:

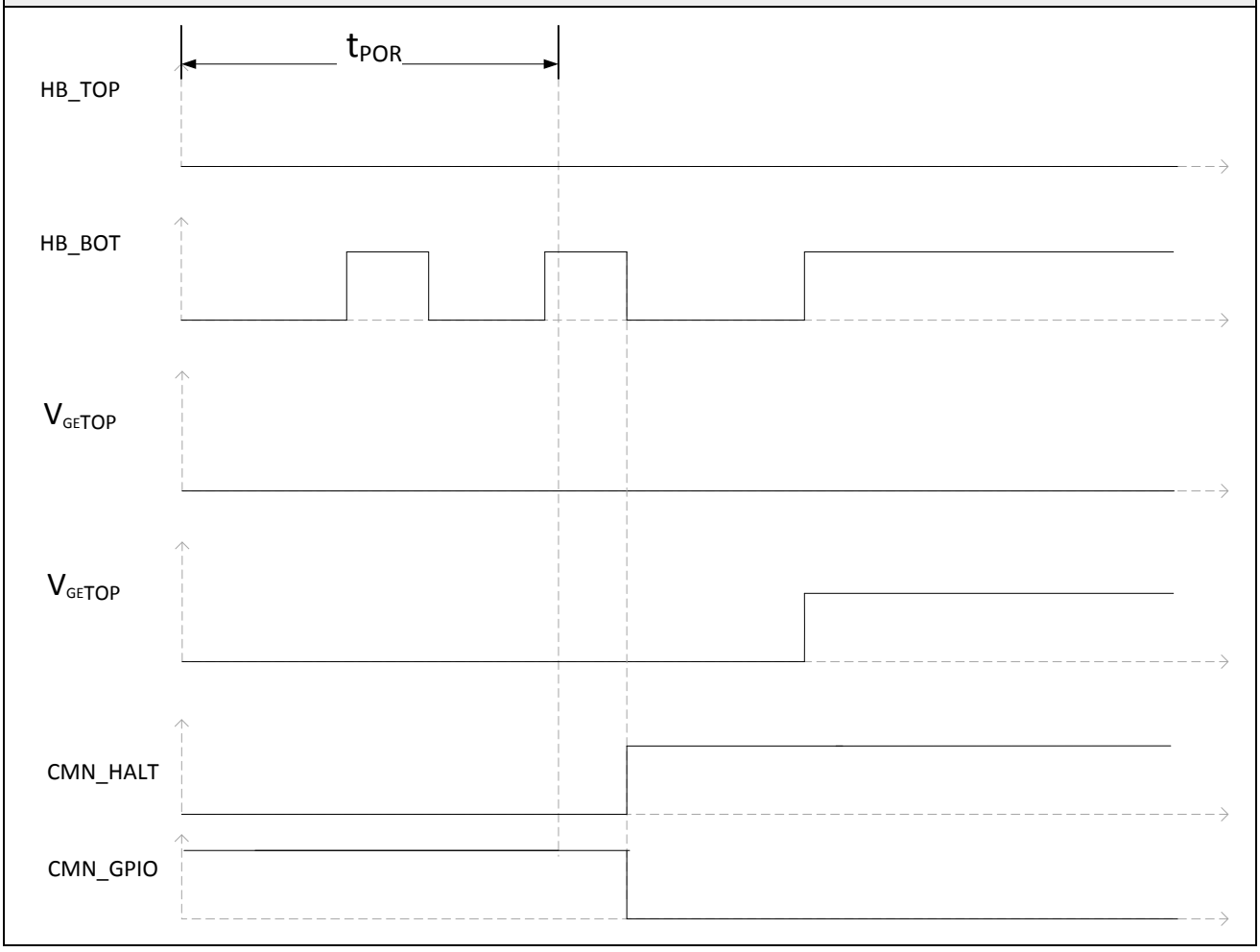
- No temperature and aging effects
- Galvanic Isolation between low (primary) and high voltage (secondary) side inclusive temperature and DC-Link voltage feedback
- High signal integrity
- High noise immunity

5.3.3 Power-On-Reset

The Power-On-Reset time is defined as t_{POR} in the SKiiP®4 data sheet.
The driver board processes a Power-On-Reset after turning on the supply voltage. During t_{POR} the HALT signal is set to LOW. Without any error present, the HALT signal will be HIGH after the Power-On-Reset is completed.

Please note: To assure a high level of system safety the TOP and BOT signal inputs must stay in a defined state (OFF state) during driver turn-on time. After the end of the power on reset, IGBT operation is permitted. The driver will stay in error mode if switching signals are applied during power on as long as the both switching signals are not LOW (see Figure 5.17).

Figure 5.17: Power-On-Reset timing diagramm



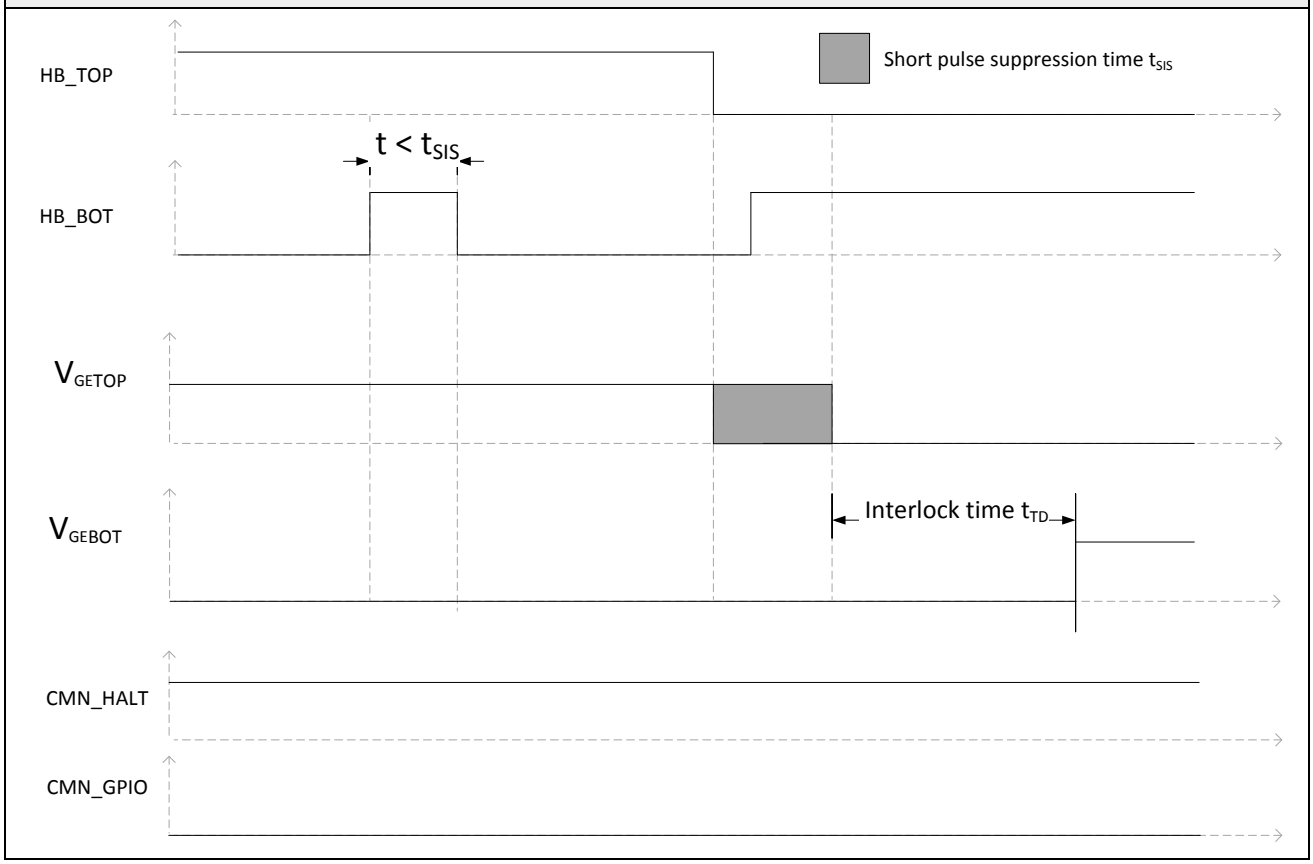
5.3.4 Interlock Dead Time Generation

The interlock dead time is defined as t_{TD} in the SKiiP®4 data sheet.
The dead time circuit prevents, that TOP and BOT IGBT of one half bridge are switched on at the same time.
It is allowed to control the SKiiP®4 by inverted pulses that means without controller dead time.
t_{TD} is not added to a dead time given by the controller (see Figure 5.18).

5.3.5 Short pulse suppression

The short pulse suppression time is defined as t_{SIS} in the SKiiP®4 data sheet.
This function suppresses short turn-on and off-pulses at the pins HB_TOP and HB_BOT of the SKiFace interface. In this way the IGBTs are protected against spurious noise which can occur due to bursts on the signal lines. If the pulse is shorter than t_{SIS}, it will be suppressed, the other chanel remains on. No error will be indicated.

Figure 5.18: Short pulse suppression



5.3.6 IntelliOff

The SKiiP®4 has two different gate turn-off paths. Both paths distinguish in the gate resistor value. The corresponding gate turn-off path will be chosen according to the actual measured AC current value. As shown in Figure 5.19 the turn-off area can be divided into:

- Hard switch-off
- IntelliOff

Figure 5.19 : Switch-off areas

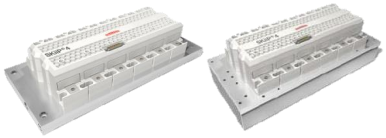
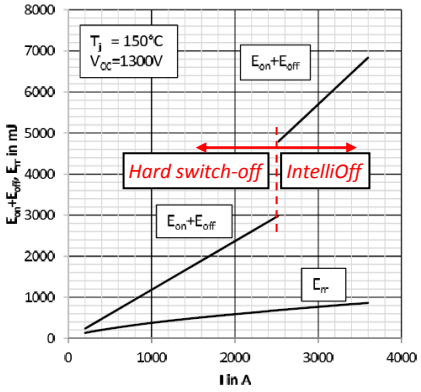
SKiiP®4 types with integrated IntelliOff function are listed in Table 5-4(⊘ not implemented, ✓ implemented)

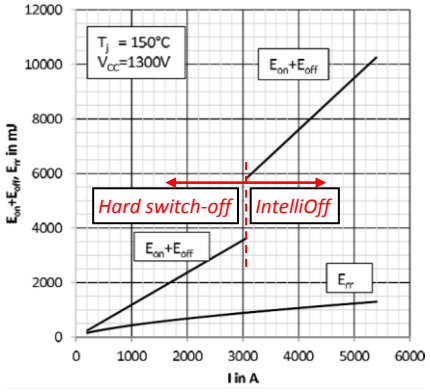
Table 5-4: IntelliOff functionality

SKiiP voltage class			
			
SKiiPxxxxGB12	⊘	⊘	⊘
SKiiPxxxxGB17	⊘	✓	✓

In the IntelliOff area the IGBT is switched-off using higher gate resistors compared to hard switch-off.

Table 5-5: Power losses due to IntelliOff



5.3.7 Failure Management

A failure caused by

- Undervoltage primary side (refer to chapter 5.3.7.2)
- Undervoltage secondary side
- Exceeding maximum switching frequency (refer to chapter 5.3.7.3)
- Overlapping of TOP/BOT switching signals (refer to chapter 5.3.7.4)
- SKiiP internal Short Circuit (refer to chapter 5.3.7.5)
- Exceeding maximum DCB-sensor/driver temperature
- DC-link overvoltage

will set the HALT signal into LOW state (not ready to operate) for the error time + at least "error memory reset time", t_{pRESET} (refer to SKiiP®4 data sheet, page 2). The IGBTs will be switched off and switching pulses from the controller won´t be transferred to the output stage. During this time the driver will check if the switching input signals HB_TOP and HB_BOT are set to LOW. If this is the case and no error is present anymore the driver will release the HALT signal. If the input signals have not been switched to LOW state the driver will pull the HALT signal to LOW (dominate) as long as the switching input signals HB_TOP and HB_BOT are not LOW. So in case of error the switching input signals HB_TOP and HB_BOT should be set to LOW within the error memory reset time t_{pRESET} and not be activated before the HALT signal is in HIGH state (see Figure 5.22).

5.3.7.1 Error delay time, $t_{d(err)}$

The error delay time is a propagation delay time of the error. This time is different for the different types of error. The exact values for the certain error types can be found in the Table 5-6.

Table 5-6: Signal characteristics of Under Voltage Protection primary side

Type of error	Error delay time, typical values
DC-Link overvoltage	160 µs
Overcurrent protection (OCP-error)	2 µs
Short circuit protection (SCP) by V_{cesat} monitoring	3 µs
DCB-sensor overtemperature	35 ms
Exceeding maximum switching frequency	6 µs

5.3.7.2 Under Voltage Protection (UVP) supply voltage

The Gate Driver board is equipped with a UVP of the supply voltage. The UVP of the primary side monitors the supply voltage Vs. Table 5-7 summarizes the trip level.

Table 5-7: Signal characteristics of Under Voltage Protection primary side

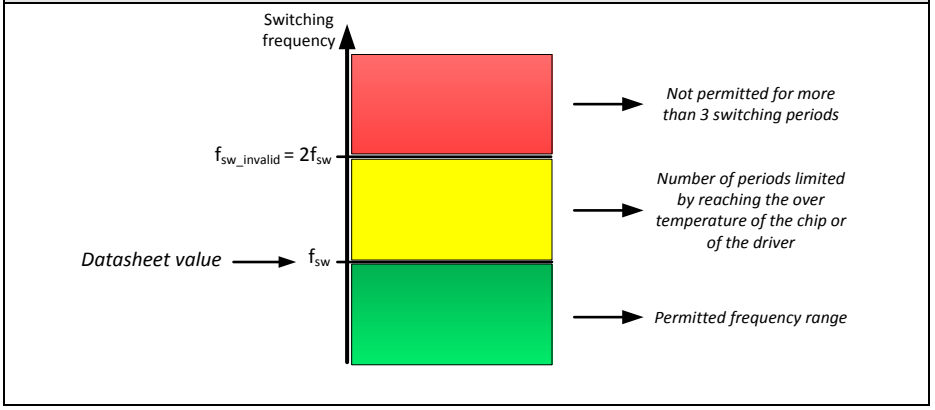
Signal Characteristics	**typ. value**
Undervoltage protection trip level	18,5V
Threshold level for reset after failure event	19V

If the supply voltage of the driver board falls below the trip level, the IGBTs will be turned off (IGBT driving signals set to LOW). The switching input signals HB_TOP and HB_BOT will be ignored and the status signal HALT changes to the LOW state. The system restarts after the error memory reset time t_{pRESET} (refer to SKiiP®4 data sheet, page 2)., if the supply voltage exceeds the threshold level for reset after failure event **and** if the switching input signals HB_TOP and HB_BOT are set to LOW.

5.3.7.3 Exceeding maximum switching frequency

The maximum switching frequency is defined as f_{sw} in the SKiiP®4 data sheet.
In order to prevent the IGBT against overheating the switching signal inputs HB_TOP and HB_BOT are monitored with respect to oscillations. The error latch will be set if the switching frequency is higher than twice the corresponding f_{sw}.
Figure 5.20 illustrates the frequency ranges.

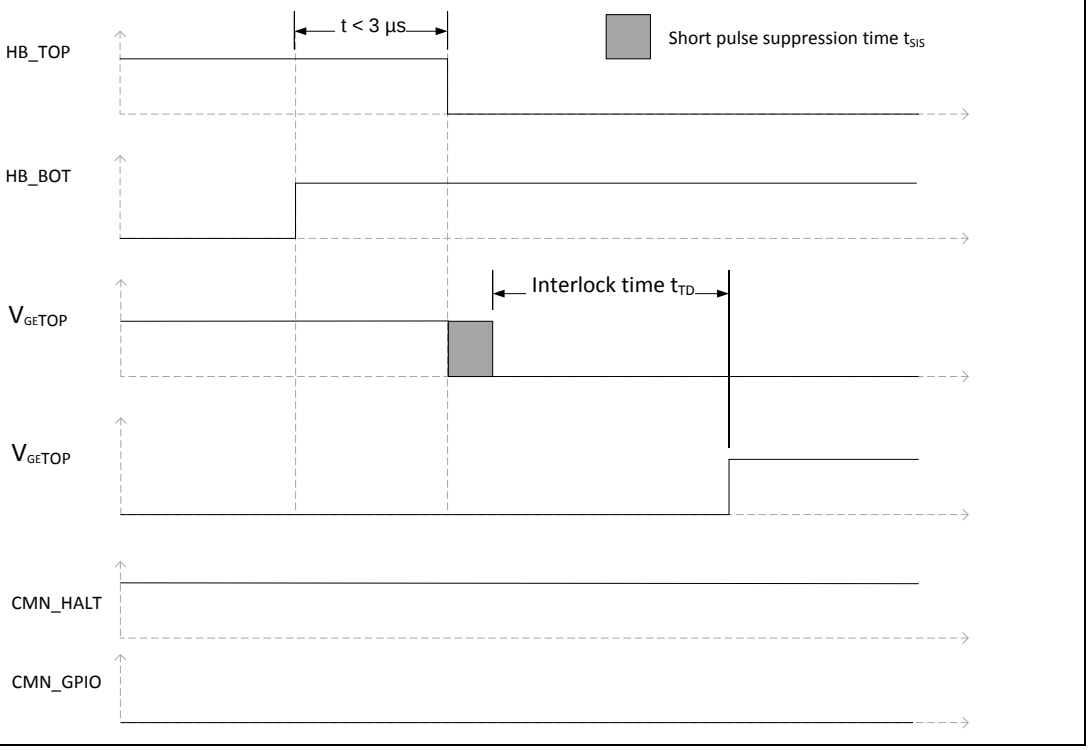
Figure 5.20: Switching frequency range



5.3.7.4 Prevention of switching signals overlapping

It is not allowed, that TOP and BOT IGBT of a half bridge are switched on at the same time. Since the switch on pulse is detected on the switching channel during the other channel is still on, the duration of the overlapping will be measured.
If the overlapping is shorter than 3 µs the switched-on channel remains on during the whole overlapping time. After the overlapping ended and the interlock time is over the other channel will be switched on. The timing diagram of the error processing in case the overlapping duration is shorter than 3µs, is shown in the Figure 5.21.

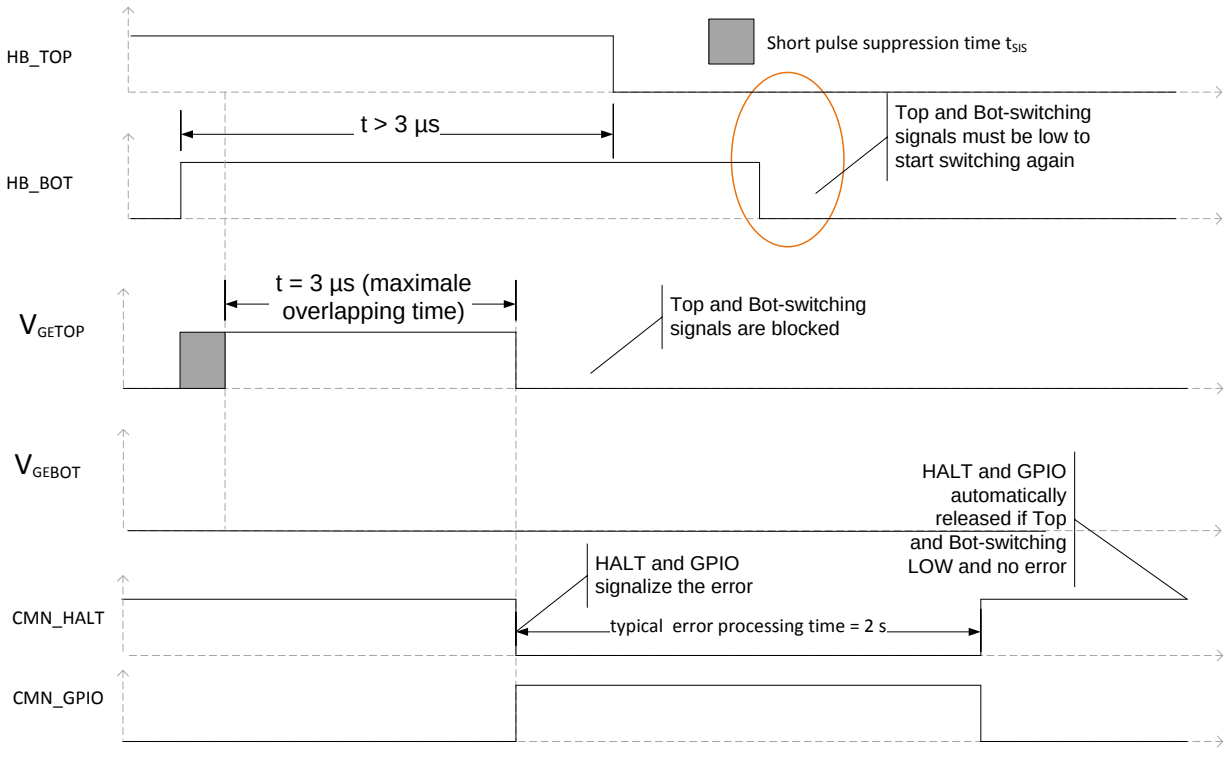
Figure 5.21: Timing diagram for the TOP/BOT overlapping error processing (t<3µs)



The timing diagram of the error processing in case the overlapping duration is longer than 3µs, is shown in the Figure 5.22. In this case both channels will be blocked. The HALT signal will be set to LOW to indicate the error.

Please note: Before continuing with switching both switching input signals HB_TOP and HB_BOT must be set to LOW.

Figure 5.22: Timing diagram for the HB_TOP/HB_BOT overlapping error processing (t>3µs)



5.3.7.5 Short Circuit Protection (SCP)

The SCP circuit is responsible for short circuit sensing. It monitors the collector-emitter voltage V_{CE} of the IGBT during its on-state. Due to the direct measurement of V_{CEsat} on the IGBT's collector potential, in case of short circuit the SCP circuit switches off the IGBTs and an error is indicated.
The Collector-Emitter Threshold Static Monitoring Voltage (V_{CEstat}) and the Collector-Emitter Threshold Static Blanking Time (t_{bl}) are given in the SKiiP®4 data sheet (page 2).

Figure 5.23: No short circuit

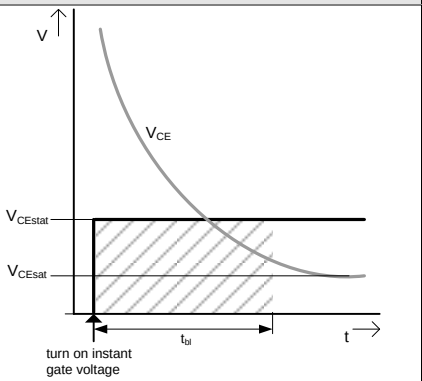


Figure 5.24: Short circuit during operation

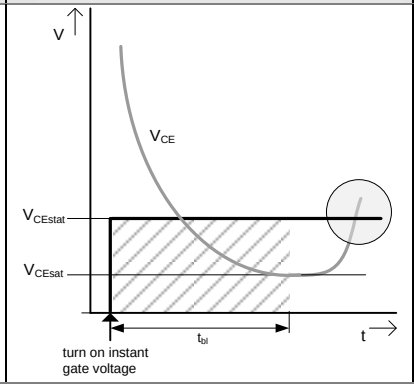
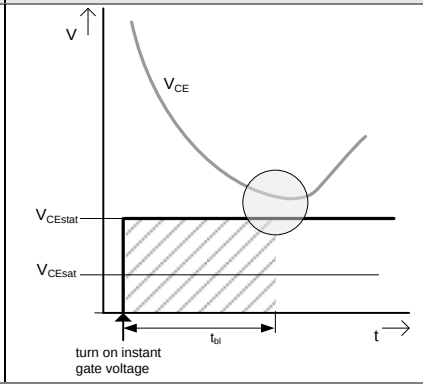


Figure 5.25: Short circuit during turn on



After t_{bl} the de-saturation monitoring will be triggered as soon as $V_{CE} > V_{CEstat}$ and will turn off the IGBT. The error memory will be set and the output HALT signal changes to LOW state.

5.3.8 Analogue signals / sensor functionality

5.3.8.1 AC-Current sensor

Each half bridge module (refer to Figure 2.1) integrates one AC-current sensor. The measured current is normalized to a corresponding voltage at the Skiface interface (see Table 5-1).

Table 5-8: Signal characteristic of current measurement

Signal Characteristics per SKiiP®4	Value		
	3-fold	4-fold	6-fold
Analogue current trip level I_{TRIPSC} HB_I = 10V	2700A	3600A	5400A
Accuracy of analogue signal @ I_{TRIPSC} over full temperature range	±3%		
Small signal bandwidth, $f0_{Iana}$	50 kHz		

Figure 5.26: Characteristic between current and the voltage at HB_I, SKiiP®4 3-fold

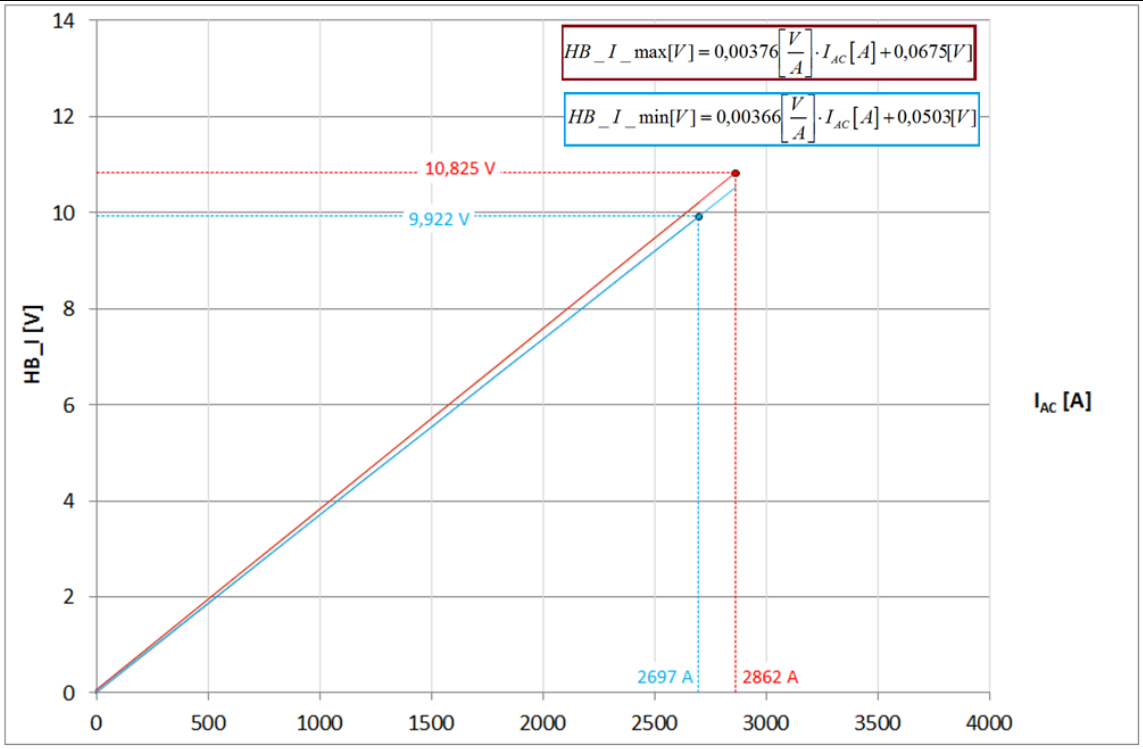


Figure 5.27: Characteristic between current and the voltage at HB_I, SKiiP®4 4-fold

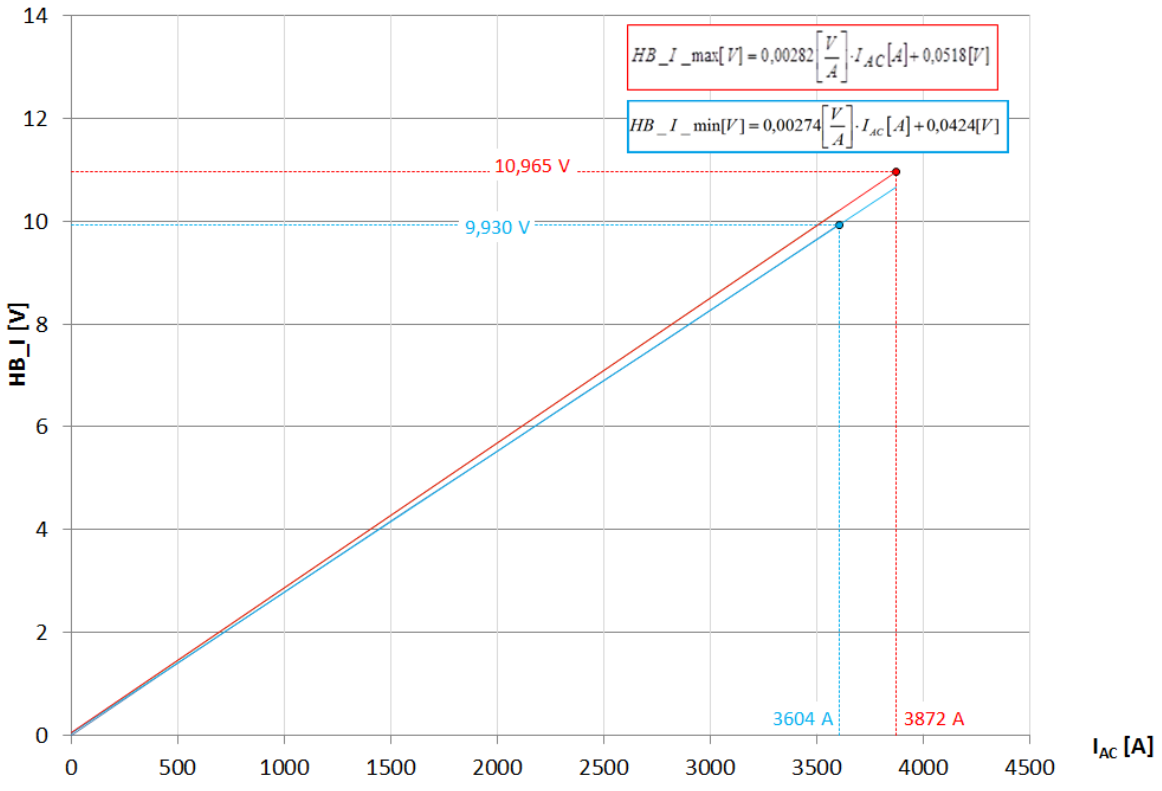
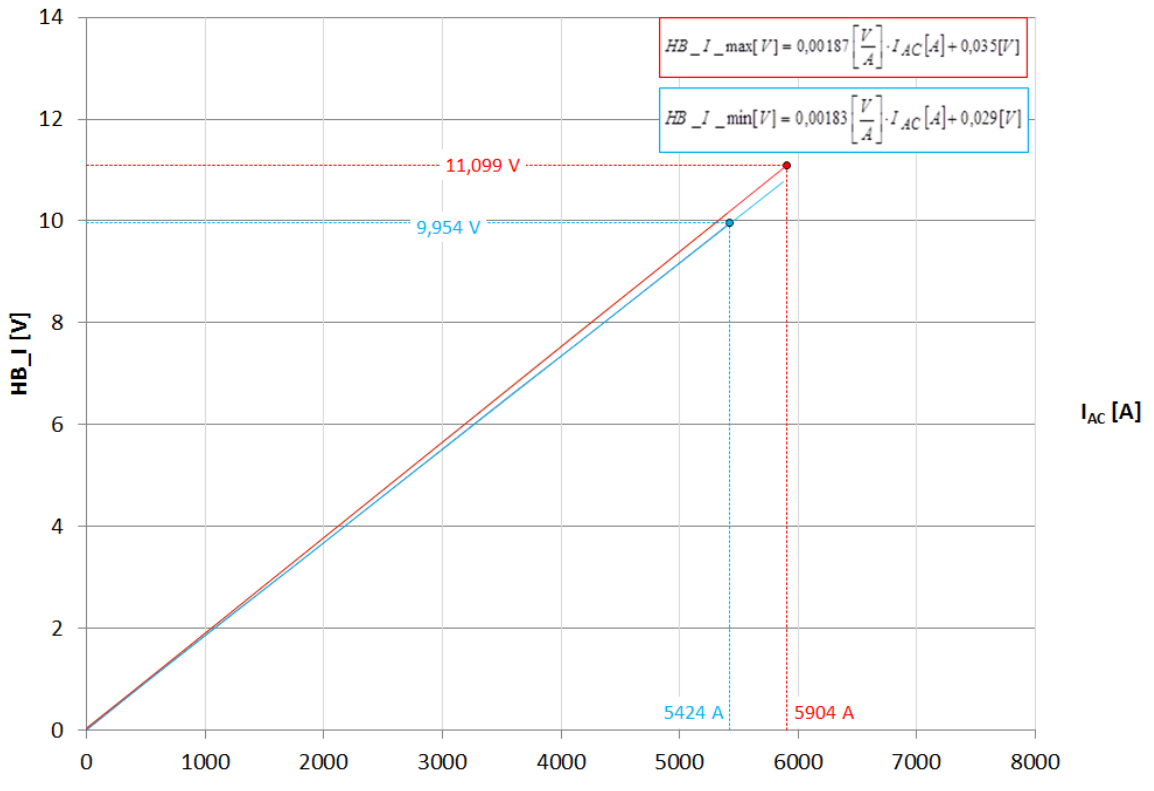
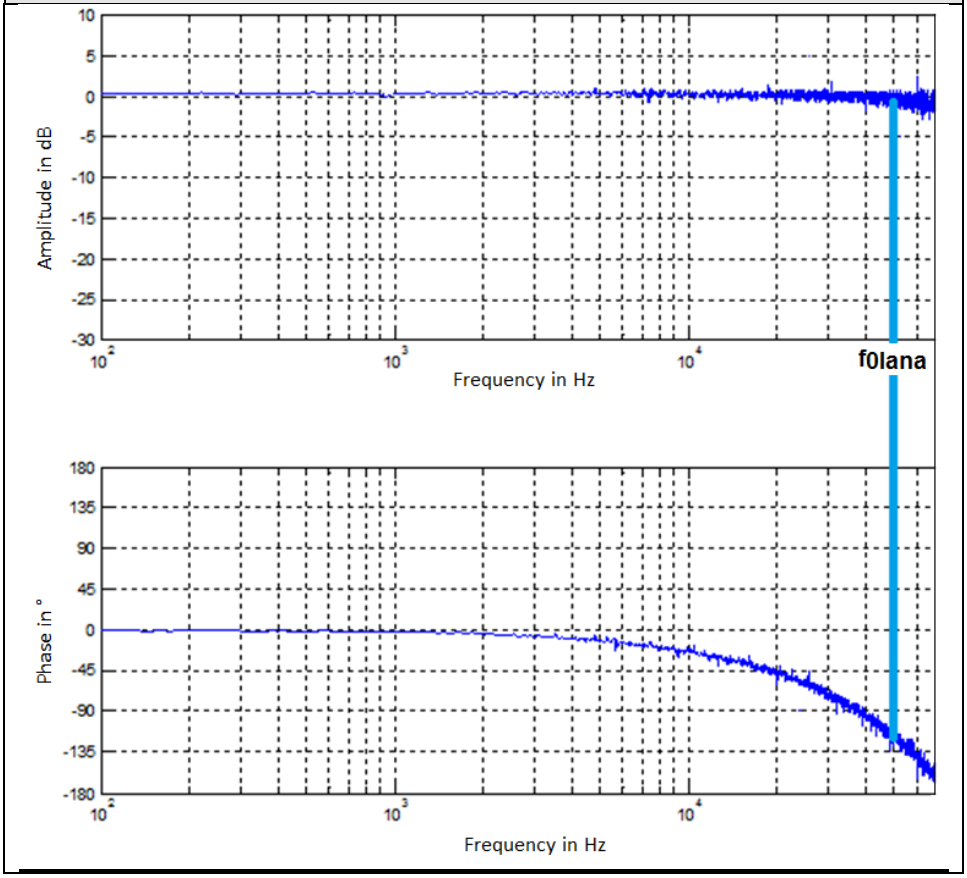


Figure 5.28: Characteristic between current and the voltage at HB_I, SKiiP®4 6-fold



The value $f0_{lana}$ given in the Table 5-8 is marked in Figure 5.29. At this frequency the amplitude is still not significantly damped.

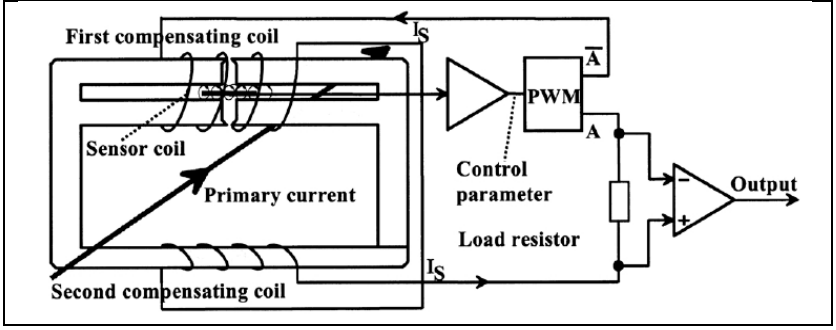
Figure 5.29: Bode diagram of the AC-current measurement at the SKiiP4 interface



Current sensor working principle

The current transformers work according to the compensation principle. The magnetic field caused by the load current is detected by a magnetic field sensor. This is not a Hall element but a small coil with a high permeable core. Due to the properties of this sensing element there is low gain and linearity failure. An electronic circuit evaluates the value of the field sensor and feeds a current into the compensation coil thus keeping the effective magnetic field to zero. The compensation current is evaluated across a burden resistor with an electronic circuit and gives an image of the load current. The SKiiP®4 current sensor uses a switch mode controller for the compensation current. This principle has remarkable lower losses than a linear controller. Figure 5.30 illustrates the compensation principle with the current sensor of SKiiP®4.

Figure 5.30: Compensation principle of SKiiP®4 current sensor



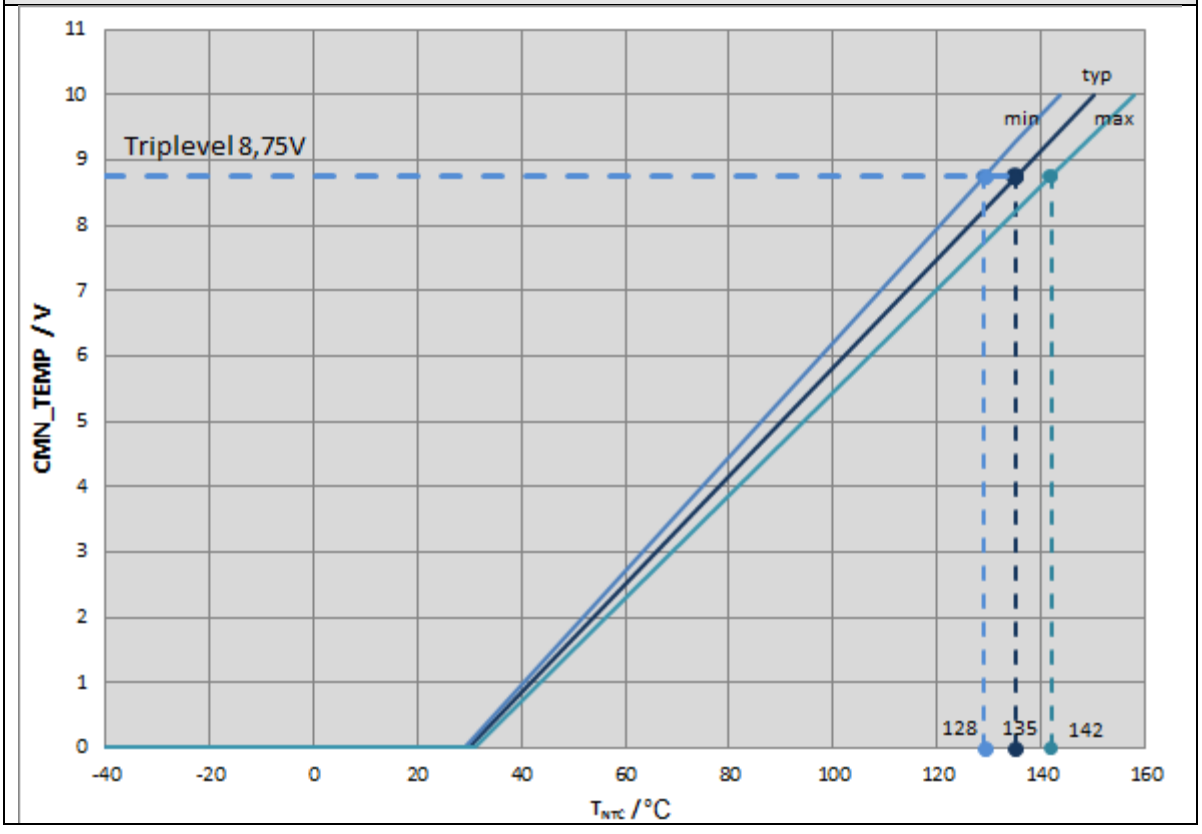
5.3.8.2 Integrated DCB-temperature sensor

The integrated DCB-temperature sensor is a chip resistor with NTC characteristic. The sensor is placed on the copper trace of the BOT IGBT (collector potential) which ensures that the measured temperature is close to the chip. The measurement circuit which is realized on the secondary side of the driver board generates an equivalent voltage which is A/D converted, transmitted to the primary side via a transformer for galvanic isolation and D/A converted on primary side. The analogue temperature signal is available on the SKiface interface (see Table 5-1) with the characteristic given below:

Table 5-9: Characteristics of the DCB-temperature sensor circuit

Temperature signal characteristics	Value
Trip level T_{trip}	135°C
Minimum measurable temperature T_{MIN}	+30°C
Analogue temperature signal CMN_TEMP @ 150°C	10V
Analogue temperature signal CMN_TEMP @ 30°C	0V
Accuracy of analogue signal @ T_{trip}	±5%
Bandwidth, f_{0Tana}	5Hz
Threshold level for reset after failure event	90°C

Figure 5.31: Characteristic between DCB-sensor temperature and the voltage at CMN_TEMP



The value $f0_{Tana}$ is given in the Table 5-9. The criteria is app. -3dB.
In case of over temperature error the system restarts after the error memory reset time t_{pRESET} (refer to SKiiP®4 data sheet, page 2)., if the DCB-temperature is lower than 90°C **and** if the switching input signals HB_TOP and HB_BOT are set to LOW.

5.3.8.3 DC-Link-Voltage Sensing

The DC-link-voltage (V_{DC}) is sensed on the secondary side of the driver board at DC plus and DC minus terminal by a differential amplifier. The output voltage of this amplifier is A/D converted, transmitted to the primary side via a transformer for galvanic isolation and D/A converted on primary side like the temperature signal. The analogue DC-link voltage signal is available on the SKiface interface (see Table 5-1) with the characteristic given inTable 5-10. This principle of the galvanic isolation has the advantage - in comparison to a measurement with high impedance resistor chain - that the primary to secondary leakage current does not increase with the number of the used SKiiPs due to the parallel connection of resistor chains.

Table 5-10: V_{DC} characteristics

V_{DC} signal characteristics	**1200V System**	**1700V System**
Analogue DC-link voltage signal CMN_DCL @ 900V	9V	6,5V
Analogue DC-link voltage signal CMN_DCL @ 1200V		9V
Accuracy of analogue signal @ V_{DCTrip} over full temperature range	±3%	
Bandwidth, f_{0Uana}	1,8kHz	

The characteristic between the DC-Link voltage and the signal on CMN_DCL for 1200V and 1700V SKiiP®4 systems can be found in the Figure 5.32 and Figure 5.33 corresponding.

Figure 5.32: DC link voltage sensor output 1200V system

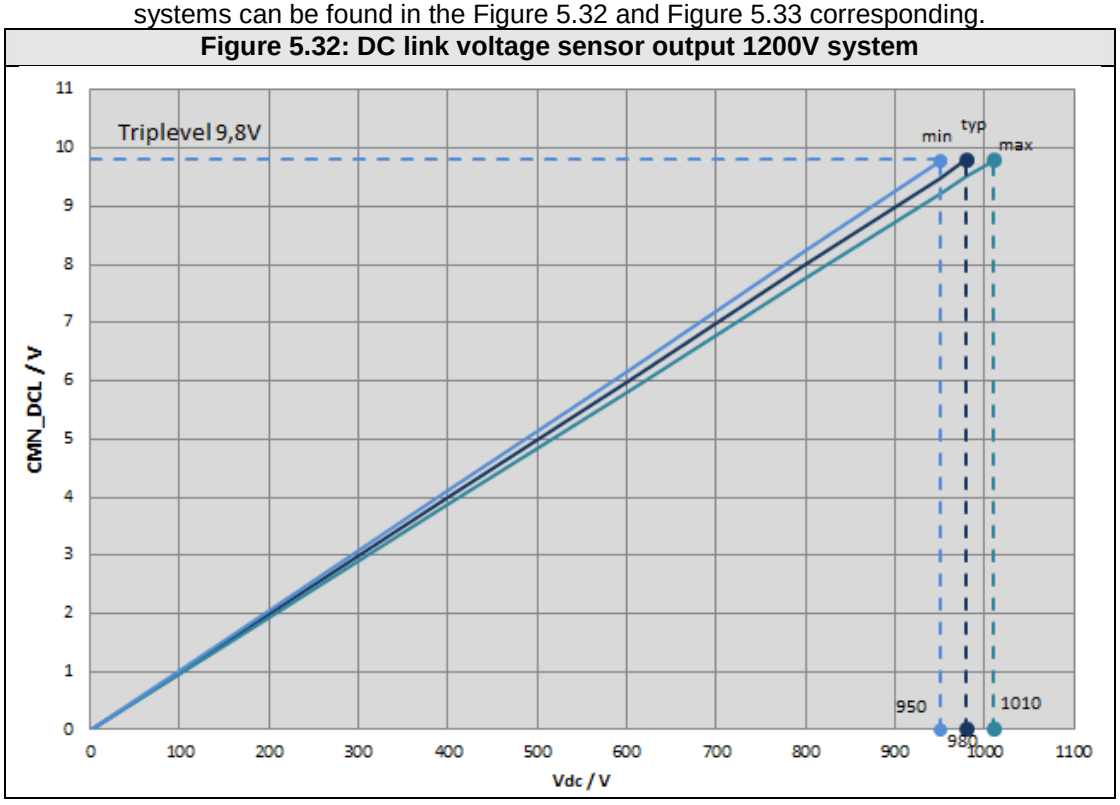
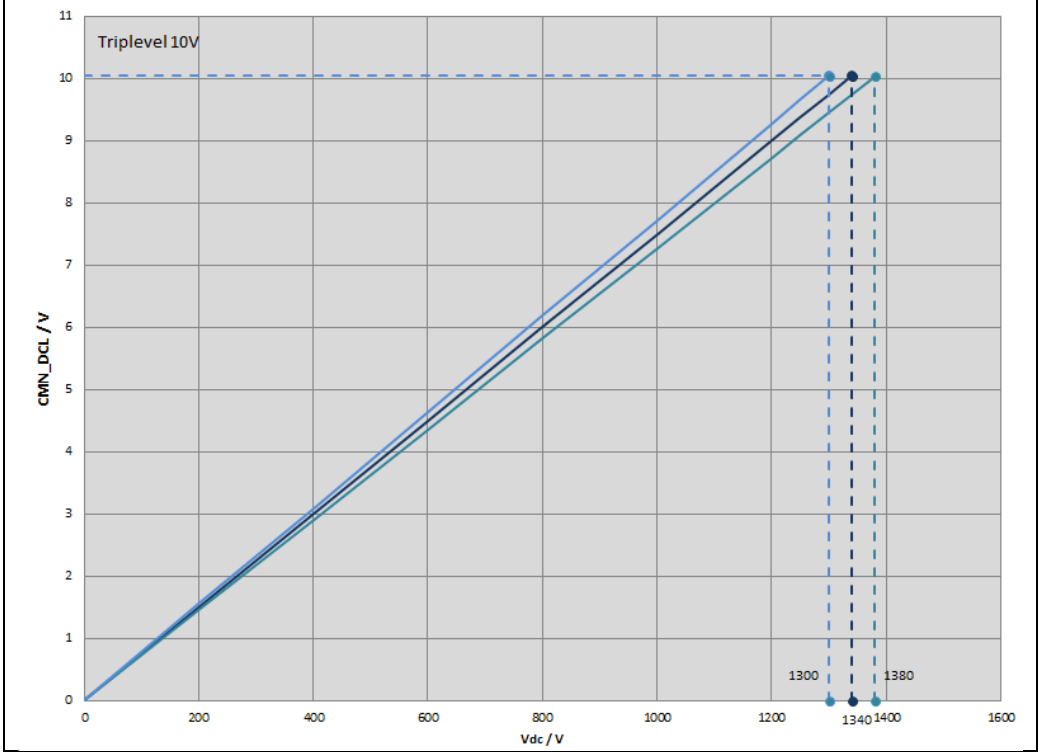
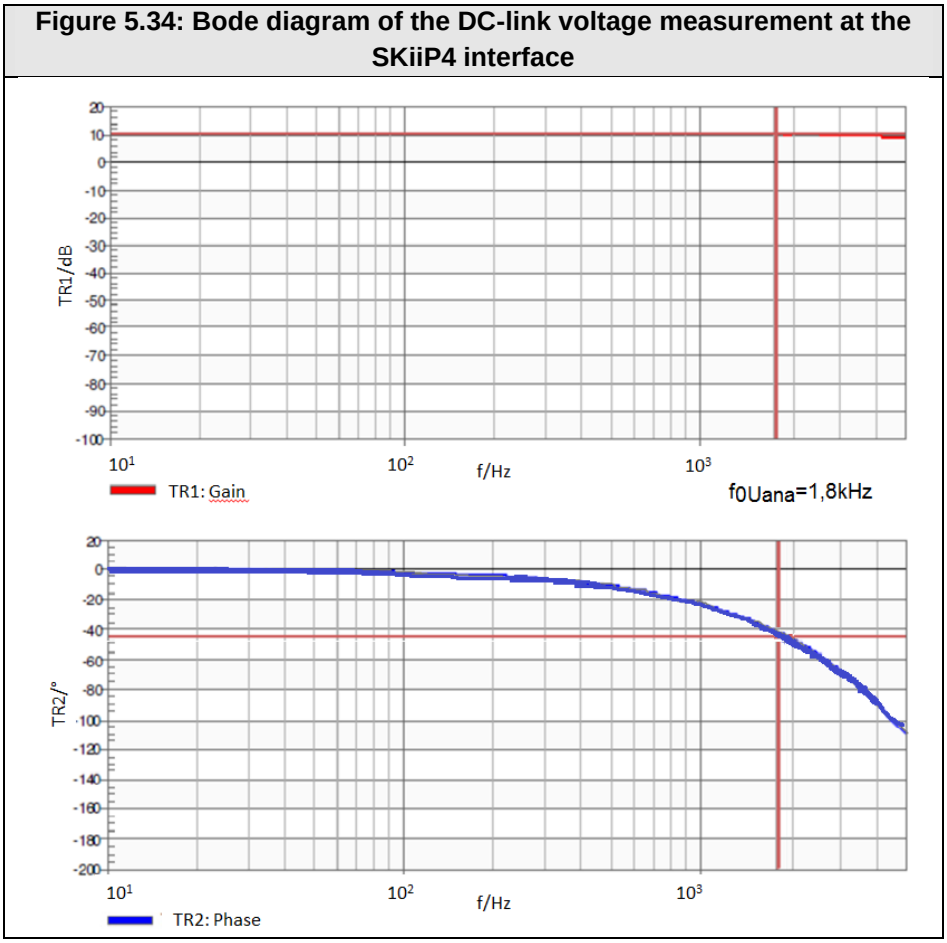


Figure 5.33: DC-link voltage sensor output 1700V system



The value $f0_{Uana}$ =1,8kHz is marked in Figure 5.34. The criteria is a -45° phase shift.
At a phase shift of -45° the amplitude is still not significantly damped.

Figure 5.34: Bode diagram of the DC-link voltage measurement at the SKiiP4 interface



6 Power terminals

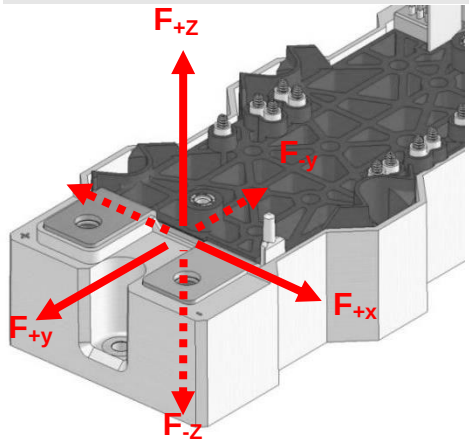
The power terminals of the SKiiP®4 are robust against external forces which may be caused by the connection of the DC-link and load cables. Nevertheless, the SKiiP module is NOT MEANT to support the DC link. The mechanical support must also be provided for the AC connection (e.g. inductor or motor cables) in order to protect the power terminals from mechanical forces and vibration stress. The maximum forces that must not be exceeded are given in Table 6-1.

Table 6-1: Maximum allowable forces to terminals

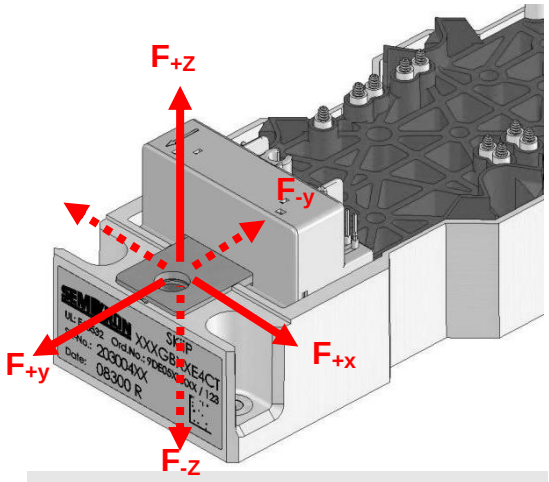
Force	Maximum allowed force [N]
F_{+x}/ F_{-x}	300
F_{+y}/ F_{-y}	300
F_{+z}/	200
F_{-z}	500

Figure 6.1: Maximum forces at the main terminals

DC-Terminals



AC-Terminal



The following should be considered in the design process:

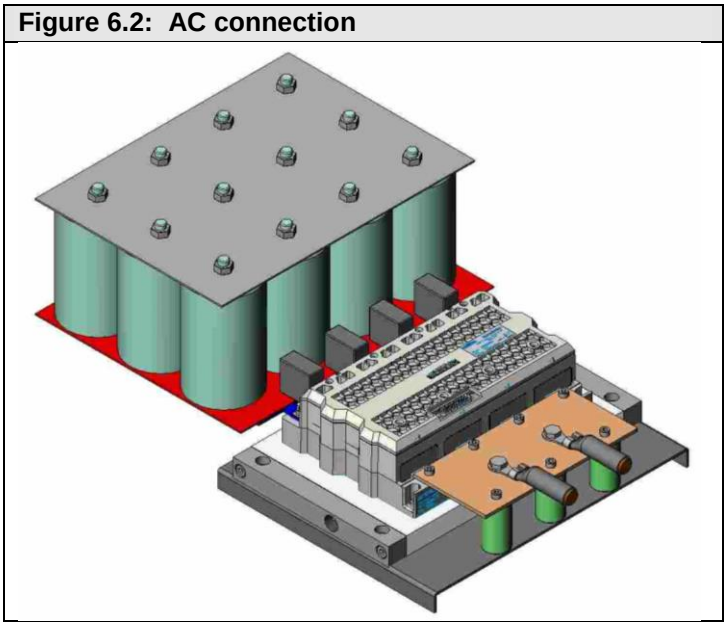
- DC connection:
  - Mechanical tolerances, especially when larger DC-links are used which are connected on more than one SKiiP
- Thermal expansion:
  - The DC-link is heated up under load and expands. This causes mechanical forces on the terminals.
- Stiffness of terminals for DC connection:
  - The connections should be soft in order to minimize the mechanical forces. This can be realized e.g. by using of tempered copper.
- Terminal hole diameter:
  - Should be large enough that the screw fits through the hole into the SKiiP connection.
- Dimensions of the DC connections:
  - Considering the heating and isolation. The terminals must not heat up snubber capacitors.

Recommended AC connection:

- Symmetrical AC connections for symmetrical current sharing between the paralleled half bridge modules. The load cable should be connected in the middle of the AC terminal and have equal distance to the each half bridge module.
- Connect a plate (e.g.copper) on all AC terminals of one SKiiP
- Cables can be connected on the same plate but it has to make sure that the cables do not apply force on the terminals (pull or push). Therefore flexible cables with stress relief should be used.
- The plate should be fixed by fixing poles. These poles shall be mounted directly on to the heat sink or a fixed frame construction and placed close to the SKiiP device.

The design has to be as depicted in Figure 6.2.

Figure 6.2: AC connection



Please note: All screws of the AC terminals must be tightened uniformly (**not one screw completely fixed before the others**) to avoid the warping.

7 Application hints

7.1 Verification of design

Measurements and calculations have to be carried out to be sure that the design works reliable. The following points have to be considered:

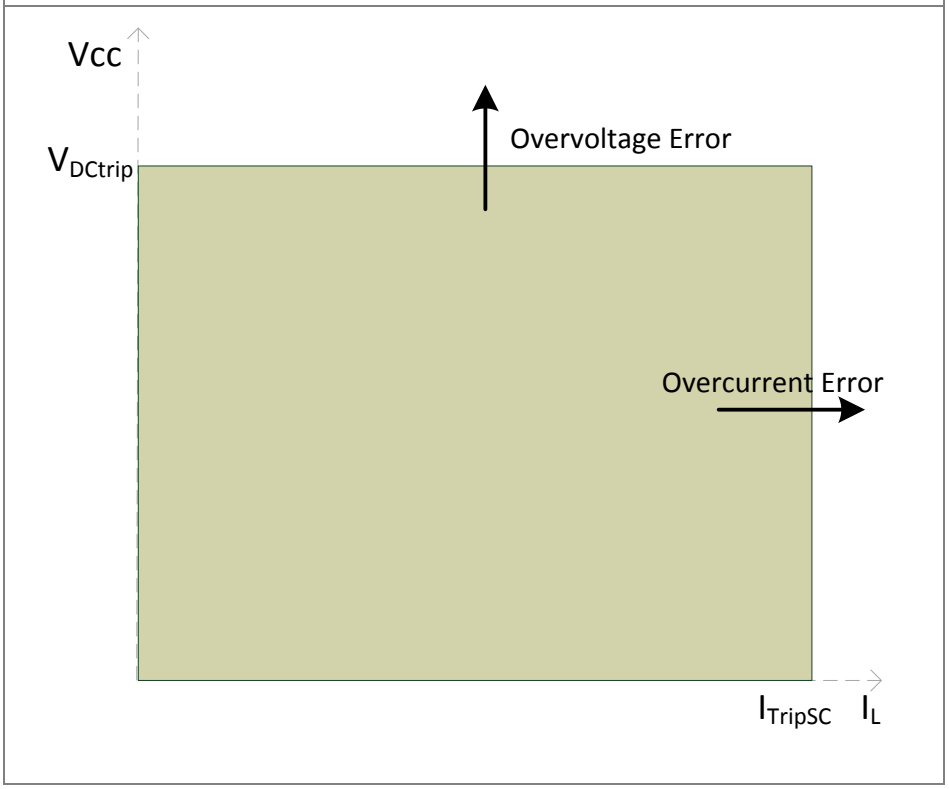
- Maximum blocking voltage V_{CES}/V_{RRM} must not be exceeded in any case (normal conditions, short circuit)
- Load current of snubber capacitors
- Current sharing between paralleled half bridge modules
- Recommended IGBT and diode junction temperatures must not be exceeded also considering overload conditions
- Environmental temperatures of driver board which affects the lifetime of the driver board electronics
- Load and temperature cycles which affect the lifetime of the power part
- Environmental conditions during operation, transport and storage
- EMC design
- Mechanical design

Besides these general points application specific conditions and requirements may be considered too.

7.2 Safe Operating Area for SKiiP®4

The Safe Operating Area for different SKiiP®4 systems is shown in the Figure 7.1. Please reffer to the correponding data sheets for V_{DCtrip} and I_{TripSC} values for concrete SKiiP®4 types.

Figure 7.1: Safe Operating Area for standard SKiiP®4



7.3 Maximum blocking voltage and snubber capacitors

The maximum blocking voltage V_{CES}/V_{RRM} which is given in the SKiiP®4 datasheet must not be exceeded. It must also be considered that IGBT switches faster if the junction temperature is low. The first countermeasure is a low inductive DC-link design to keep the overvoltage on the semiconductor low. In addition, snubber capacitors are recommended, which should be mounted directly on the DC-link terminals of each half bridge module. Application note AN-7006 “Peak voltage measurement and snubber capacitor specification” provides information how to perform the tests and to select the snubber capacitors. The following snubber capacitors have been designed for SKiiP®4. But nevertheless it has to be validated by testing that the capacitors are compatible with the design and will not be overloaded.

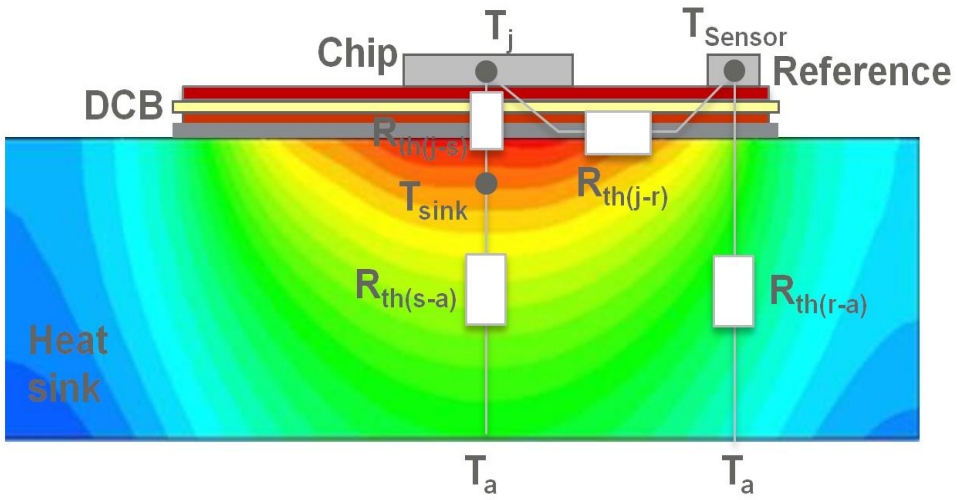
Table 7-1: Snubber capacitors for SKiiP®4

Capacitance / DC voltage	For use with
680 nF / 1000V	1200V device
330 nF / 1600V	1700V device

7.4 Definition of Thermal Resistance

Thedefinition of the thermal resistances given in the SKiiP®4 datasheet are shown in the Figure 7.2.

Figure 7.2: Definition of thermal resistances



T_j	**junction temperature of the hottest chip**
T_{sensor}	**DCB-sensor temperature**
T_{sink}	**heat sink temperature in a drill hole 2mm underneath the chip**
T_a	**ambient temperature (coolant air or liquid)**
$R_{th(j-r)}$	**thermal resistance between junction and reference**
$R_{th(j-s)}$	**thermal resistance between junction and heat sink**
$R_{th(s-a)}$	**thermal resistance between heat sink and ambient**
$R_{th(r-a)}$	**thermal resistance between reference and ambient**
P_{losses}	**Power losses of the chip**

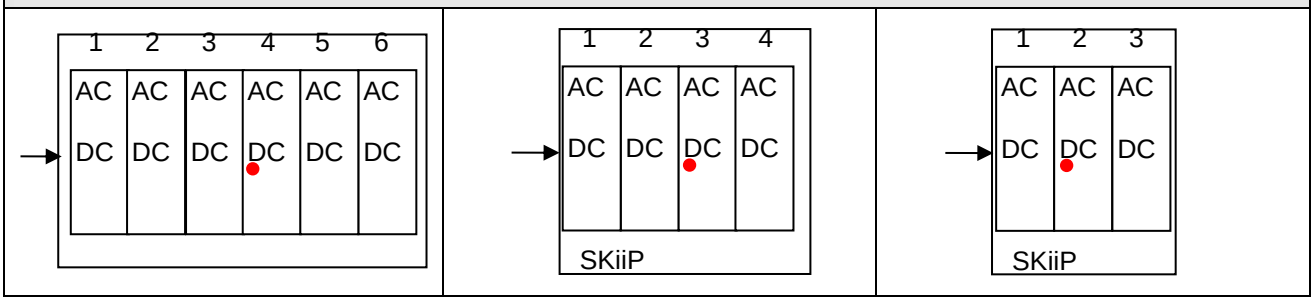
In general, the thermal resistance between two points 1 and 2 is defined according to following equation:

$$R_{th(1-2)} = \frac{\Delta T}{P_{losses}} = \frac{T_1 - T_2}{P_{losses}}$$

The data sheet values for the thermal resistance are based on measured values. The point of the temperature measurement has a major influence on the thermal resistance because of a temperature profile between the different chip positions and across the heatsink surface.
The reference points for SKiiP®4 systems are: virtual junction temperature of the hottest chip (T_j); heat sink temperature underneath the hottest chip (T_{sink}) and DCB-sensor temperature (T_{sensor}). A principle sketch with

the positions is shown in Figure 7.1. The values for $R_{th(j-s)}$, $R_{th(s-a)}$ and $R_{th(j-r)}$ are calculated from these temperatures. SKiiP modules have no base plate, therefore the case temperature T_C can not be measured without disturbance of the thermal system and the thermal resistance $R_{th(j-c)}$ cannot be given. T_{Sink} is measured in a drill hole 2mm underneath the heatsink surface. The 2 mm distance guaranties a low disturbance of the thermal path and a minimum effect of heat sink parameters like size, thermal conductivity, cooling medium etc.
The temperature sensor is located between IGBT and diode chips on the same DBC copper layer at high voltage potential. This ensures an excellent thermal coupling between both power semiconductors and sensor and furthermore a short reaction time on changes in power dissipation.
Only one of the temperature sensors is monitored by the Gate driver. The monitored sensor is in the middle of the SKiiP (refer to Figure 7.3). The protection level is matched to the maximum operation temperature of the power semiconductors.
During operation there will be a temperature profile along the heatsink from cool at the inlet of the coolant to warm at the outlet.

Figure 7.3: Sensor position in SKiiP®4 GB (6fold, 4fold, 3fold) with proposed cooling (water inlet) direction



SKiiP®4 are equipped with high performance heat sinks. The data sheets contain transient thermal data referenced to the built-in temperature sensor. This allows the calculation of junction temperature Tj, if the generated losses are known. The thermal resistances given in the data sheets represent worst case values.
Evaluation of thermal impedance:

- Junction to sensor

$Z_{th(j-r)} = \Sigma R_{th(j-r)n} * (1-e^{-t/Tn})$, n=1,2,3,….

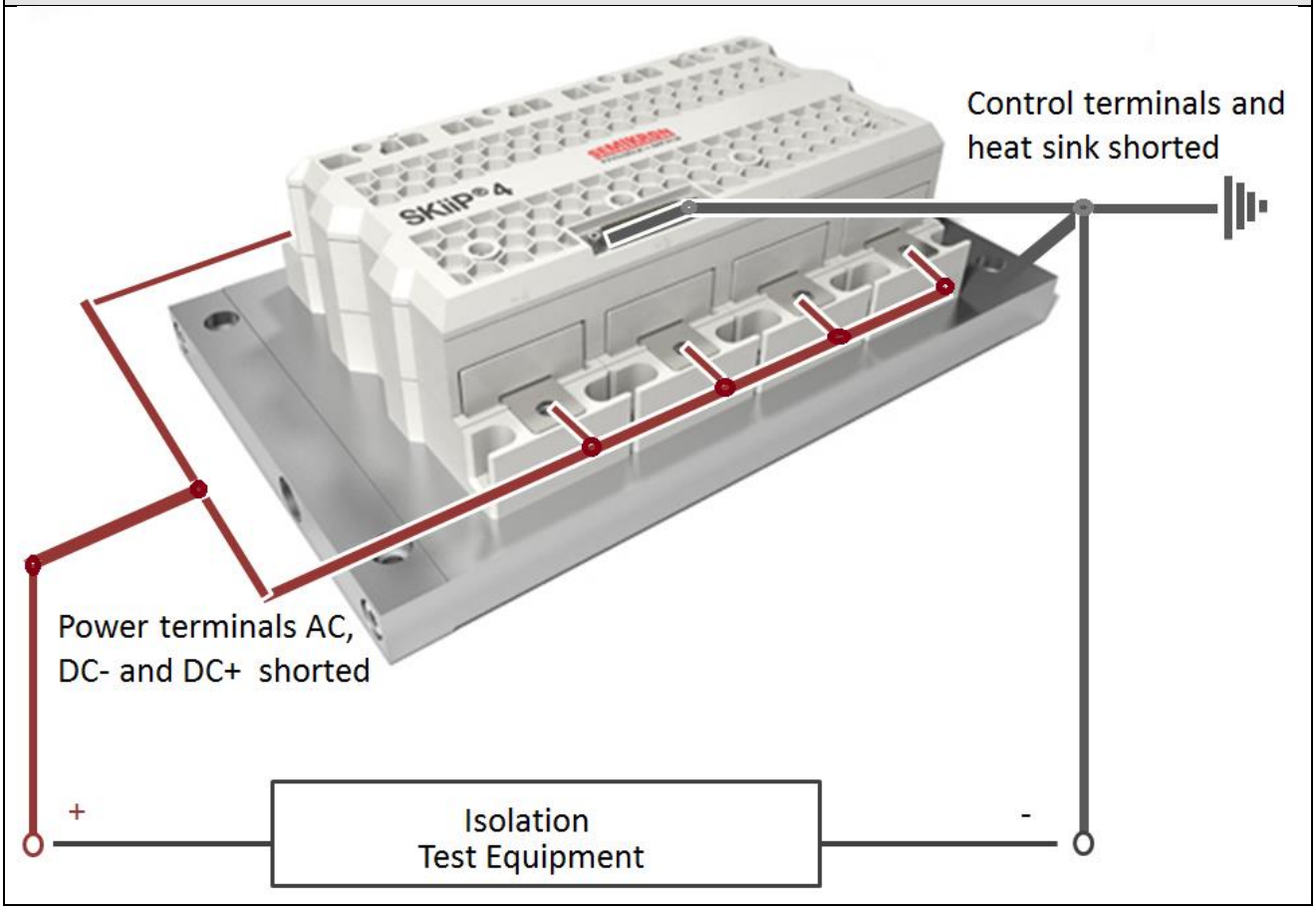
- Sensor to ambient
- $Z_{th(r-a)} = \Sigma R_{th(r-a)n} * (1-e^{-t/Tn})$, n=1,2,3,….

Please note: The values for transient thermal impedance given in the data sheets ($Z_{th(j-r)}$) are only valid together with the SEMIKRON standard heat sinks and under conditions given in the data sheets. The usage of these values for other heat sinks/conditions might cause deviations in calculation of thermal resistance!

7.5 Isolation voltage test (IVT)

During production test the isolation voltage of 5600Vdc (1700V devices) or 4300Vdc (1200V devices), DC, each polarity, is applied to the 100% of SKiiP-systems for 1s with test set up shown in the Figure 7.4 These values are also available in the corresponding datasheets.

Figure 7.4: Graphic presentation of the electrical connections by the IVT procedure



The polarity change (whereby heat sink is always grounded) is only possible if the customer uses a galvanically isolated test control device. Otherwise the plus and minus pole of the isolation test control device will be shorted.

Please note: Because of the safety measures during and after the test procedure the heat sink should be grounded: if the DUT fails with an arcing and if the test control device recognizes it and disconnects from the DUT, it is possible the DUT is still electrically charged. In this case it would be dangerous to touch the DUT after the test procedure. In addition to this without grounding the test voltage could drift and the voltage to ground will be even higher than the nominal test voltage.

All isolation voltage tests must be performed at an ambient temperature of 15…35°C, a relative humidity of 45…75% and an atmospheric pressure of 860…1060 hPa. The norms define no certain leakage current value, thus the isolation test (dielectric test) is considered passed if no electrical breakdown has occurred, i.e. small leakage currents that occur are irrelevant.

There are two forms of an isolation damage:

1. Fully breakdown (according the norms)
2. High leakage current (not according the norms!)

According to the corresponding norms it is required to do an IVT with AC voltage. Despite of this the IVT with DC voltage is recommended because in case of AC IVT the high leakage currents lead to the uncertain identification of the isolation problems.

It is recommended to ramp up the isolation voltage with 10kV/s. Faster ramp up leads to capacitive leakage currents and could cause the faulty activation of the isolation test control unit. Slower ramp up leads to the longer testing time. The count of the test time 1s, specified in the data sheet, begins after ramp up of the full isolation voltage. The isolation voltage could be switched off without a ramp down. After finishing the test it must be checked that the DUT is not charged anymore.

Please note: The isolation test voltage should not be greater than necessary for the application and the corresponding standards.

The isolation measurement is performed in two steps:

1. high voltage isolation test
2. repeated isolation test

The high-voltage isolation test and repeated test of an isolation barrier can degrade isolation capability due to partial discharge. During the IVT since the isolation voltage is applied the partial discharge starts after the voltage goes beyond the partial discharge inception voltage. The higher and the longer the voltage value is applied, the stronger the damage of the isolation through the partial discharge will be. Thus each IVT leads to the weakening of the isolation. The partial discharge in the DCB doesn't lead to the weakening of the isolation, because the ceramic is resistant to the partial discharge. First of all the organic materials (plastic), e.g. circuit boards and compound of transducers, will be damaged.
Since every isolation test may cause premature damage to the module as a result of partial discharge, the number of tests should be kept low. If they can not be avoided, however, a regeneration time of at least 10 minutes must be complied with between 2 tests and the repeated isolation voltage tests should be performed with reduced voltage. The test voltage must be reduced by 20% for each repeated test.

Please note: The F-option must be removed during the IVT (mounting instruction on request). Then the normal test procedure as above described should be done.

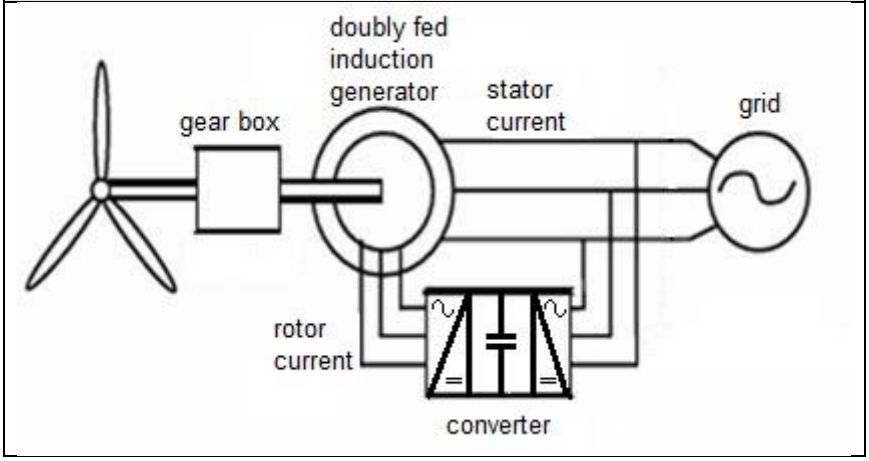
7.6 Current sharing between paralleled half bridge modules

When the IGBT is switched on the current is commutated over the paralleled IGBT half bridge modules. The busbar design has to be symmetrical to make sure that the current sharing is equal. Unequal current sharing can overload single
half bridge modules and leads to imbalance during switching off which can finally destroy the power section. Symmetrical AC and DC-link design leads to equal stray inductances between the half bridge modules which ensures equal commutation and current sharing. Each half bridge module has to have the same stray inductance to the DC-link capacitors.
The recommended AC connection is shown in Figure 7.13.The current sharing should be measured in the design phase by "double pulse testing" (see AN-7006) and in the final design under real operation conditions. This can be done e.g. by Rogowski current sensors which are located around the DC+ and DC- terminals.

7.7 FRT (Fault Ride Through) - Function

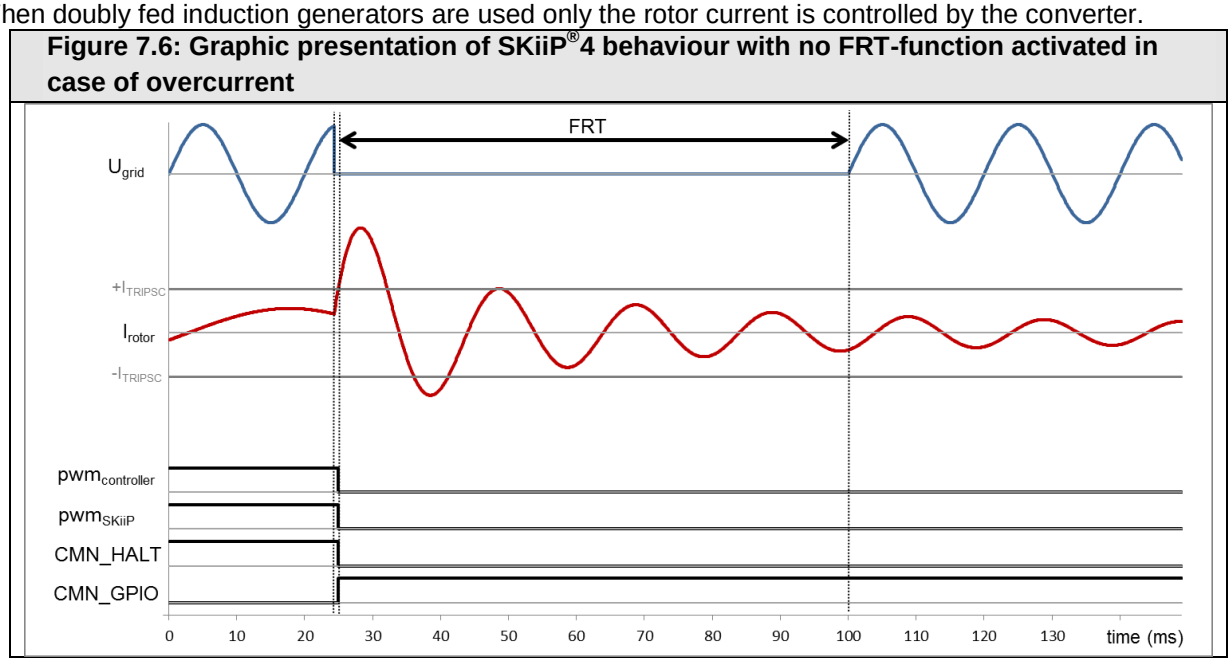
A typical SKiiP®4-application is a converter for wind turbines. It is state of the art that turbines must fulfill grid code requirements for the connection to the electric power system. Such requirements are known as Fault Ride Through (FRT) or Low Voltage Ride Through (LVRT).

Figure 7.5: Graphic schematic of the wind mill



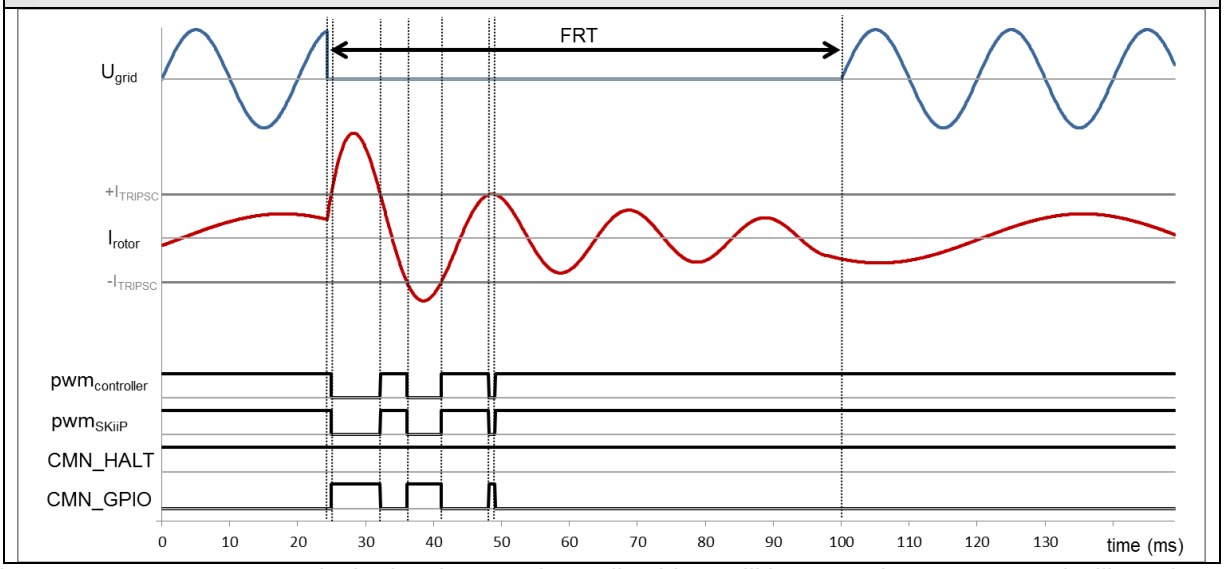
When doubly fed induction generators are used only the rotor current is controlled by the converter.

Figure 7.6: Graphic presentation of SKiiP®4 behaviour with no FRT-function activated in case of overcurrent



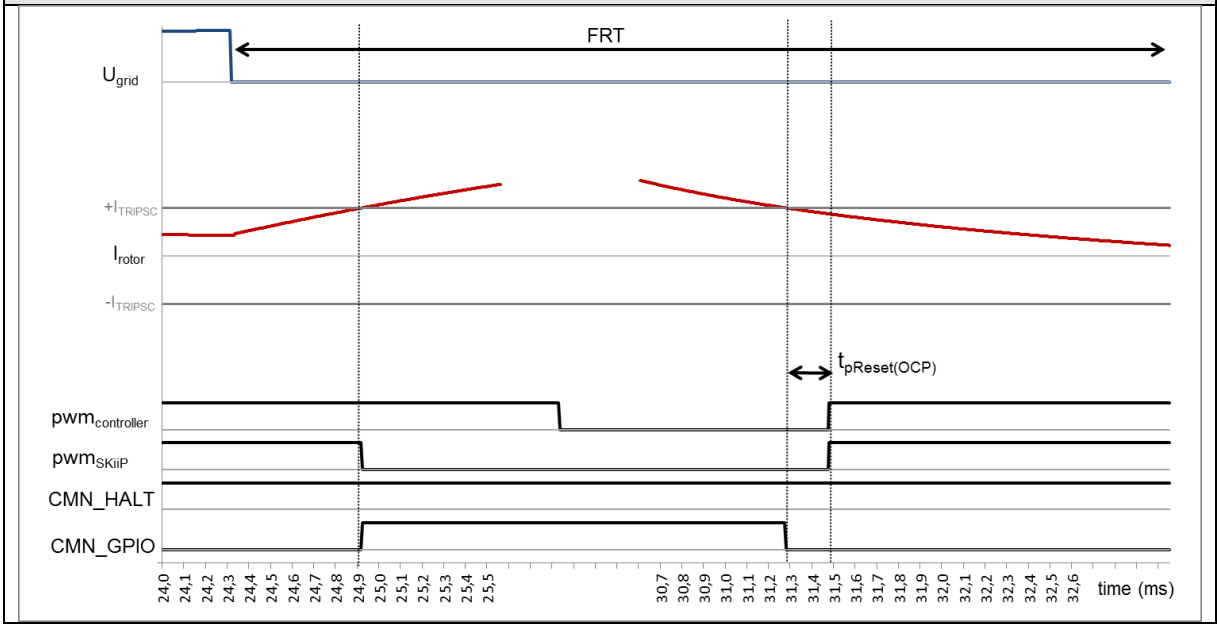
In case of an FRT or LVRT the rotor current can increase to levels higher than the overcurrent trip level of the SKiiP (I_{TRIPSC}) and the SKiiP will trip. Consequentially the PWM of the IGBTs (pwm_{SKiiP}) is interrupted by the SKiiP-driver itself regardless of whether the PWM from the customer controller ($pwm_{controller}$) is running. The SKiiP-driver sets the CMN_HALT-signal to LOW and the CMN_GPIO-signal to HIGH. The interrupt of the pwm_{SKiiP} is released after the error memory reset time t_{pRESET} has elapsed and if the switching input signals HB_TOP and HB_BOT are set to LOW. In most cases t_{pRESET} is too high to fulfill the grid code requirements.
If the FRT-function is activated the error-handling of the SKiiP will be changed and the grid code requirements can be reached. In this case CMN_GPIO will not be the inverted CMN_HALT signal anymore. An overcurrent trip will never set CMN_HALT to LOW and it is never stored in the SKiiP error memory.

Figure 7.7: Graphic presentation of SKiiP®4 behaviour with FRT-function activated in case of overcurrent



If the rotor current I_{rotor} exceeds the level I_{TRIPSC} the SKiiP-driver will interrupt the pwm_{SKiiP} and will set the signal CMN_GPIO to HIGH as long as I_{TRIPSC} is exceeded. The $pwm_{controller}$ must be turned off. After a period $t_{pReset(OCP)}$ of 200µs which starts after I_{rotor} is below I_{TRIPSC} and $pwm_{controller}$ is turned off, the SKiiP is enabled to start switching as long as the overcurrent trip level is not exceeded again.

Figure 7.8: Graphic presentation of the driver processing in FRT-case



The freewheeling diodes conduct the rotor current I_{rotor} during the period of blocked pwm_{SKiiP}. The user must take care that the diodes will not be overloaded thermally in this time or later on, because the SKiiP overcurrent protection is deactivated and the thermal protection is not able to protect the diodes fast enough. Thermal calculations or simulations are necessary to confirm that the SKiiP diodes will not be overloaded. The activation of FRT-Function could be easy made by customer via CAN-Bus interface. Please see the CAN manual documentation for further details.

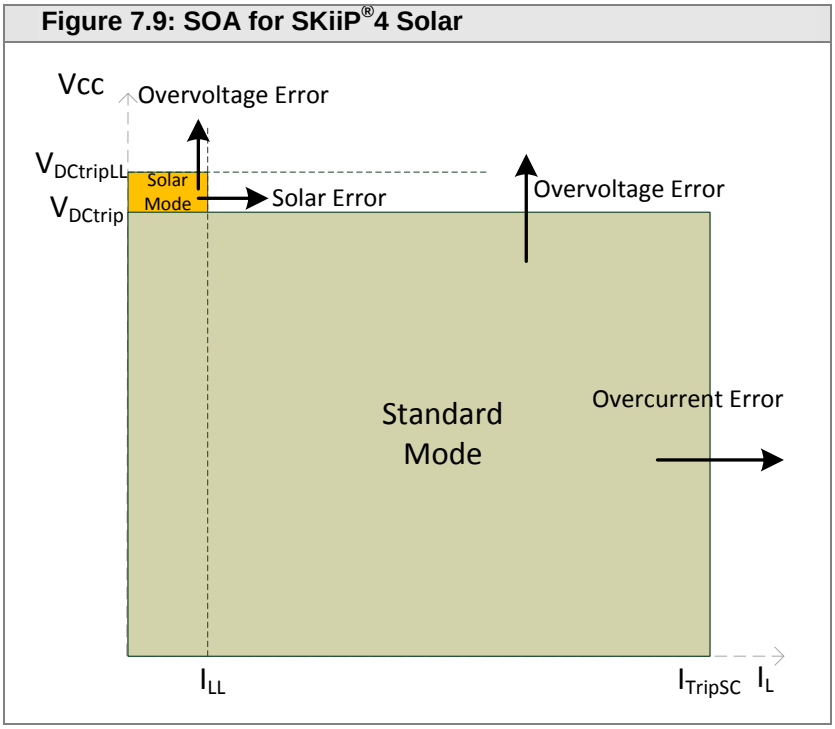
7.8 Solar function

For effective operation of the SKiiP®4 during start up phase, a higher DC-link voltage trip level must be available for low load currents in comparison to standard application. Special modification of the existing SKiiP®4 1200V type was created to fulfill requirements of the solar market.

Please note: The solar function cannot be activated via CAN, special SKiiP®4 type must be ordered. It is only available for 1200V type SKiiP®4 systems.

The Safe Operating Area (SOA) diagram for SKiiP®4 solar is available in the Figure 7.9. Whereas the SOA for standard SKiiP®4 (shown in the Figure 7.1) is limited by over voltage trip level V_{DCtrip} and over current trip level I_{TRIPSC} , the SOA of Solar SKiiP®4 has an additional area above V_{DCtrip} limited by the low load current I_{LL} and a higher over voltage trip level $V_{DCtripLL}$. This operation mode is called “solar mode” and is marked orange in the right diagram of Figure 7.9. Parameters I_{LL} and $V_{DCtripLL}$ are given in the data sheets SKiiP®4 Solar.

Figure 7.9: SOA for SKiiP®4 Solar



The operation modes for SKiiP®4 solar are listed in the Table 7-2.

Table 7-2: Operation modes SKiiP®4 solar

Operation mode	DC-voltage	Load current	Processing
Standard mode	$V_{DC} < V_{DCtrip}$	$I_{Load} < I_{trip}$	Hard Switch-off
Solar mode	$V_{DCtrip} < V_{DC} < V_{DCtripLL}$	$I_{Load} < I_{LL}$	Switch off with IntelliOff
Error mode		$I_{Load} > I_{trip}$	Switch off with IntelliOff, over current error indicated
	$V_{DCtrip} < V_{DC} < V_{DCtripLL}$	$I_{Load} > I_{LL}$	Switch off with IntelliOff, solar mode error indicated if previous mode was solar mode
	$V_{DCtrip} < V_{DC} < V_{DCtripLL}$	$I_{Load} > I_{LL}$	Switch off with IntelliOff, over voltage error indicated if previous mode was standard mode.
	$V_{DC} > V_{DCtripLL}$		Switch off with IntelliOff, over voltage error indicated

In case SKiiP®4 is in solar mode (see Table 7-2) and at DC-Link voltage $V_{DC} > V_{DCtrip}$ the load current I_{Load} exceeds $I_{LL,}$ the solar mode error will be indicated. In this case SKiiP®4 comes into error mode: the SKiiP-driver sets the CMN_HALT-signal to LOW and the CMN_GPIO-signal to HIGH. The interrupt of the operation mode is released after the error memory reset time t_{pRESET} has elapsed and the switching input signals HB_TOP and HB_BOT are set to LOW.
The solar mode error can be read out by means of CANopen diagnostic. In the case of this error, both error bits 13 (over current) and 14 (DC-Link error) will be set. Please see the CANopen Object Dictionary Rev.6 chapter 3.8. “Error recording” for more details.
Snubber capacitors must be used to avoid the exceeding of the maximum blocking voltage V_{CES}/V_{RRM} which is given in the SKiiP®4 datasheet. Please see the Chapter 7.5 for further information.
For safe operation the interlock time t_{TD} is increased to the 4,5µs in the solar mode (See the diagram of Figure 7.9).

Please note: The load must be connected symmetrically and the load inductivity must be not less than 6µH.

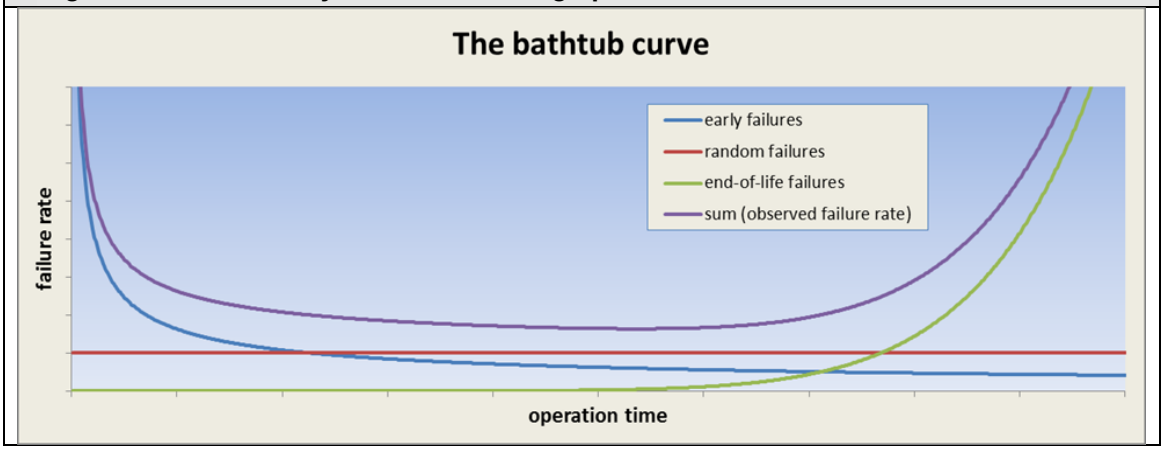
The deactivation or change of the DC-Link trip level via CAN is not possible for SKiiP4 Solar.
The activation of FRT-Function via CAN is possible (Please see CANopen Object Dictionary Rev.6).

7.9 Recommended temperature rating

Please note: The compliance of temperature characteristics recommended in this chapter are extremely important for the SKiiP®4 reliability and therefore for the long life time of the product.

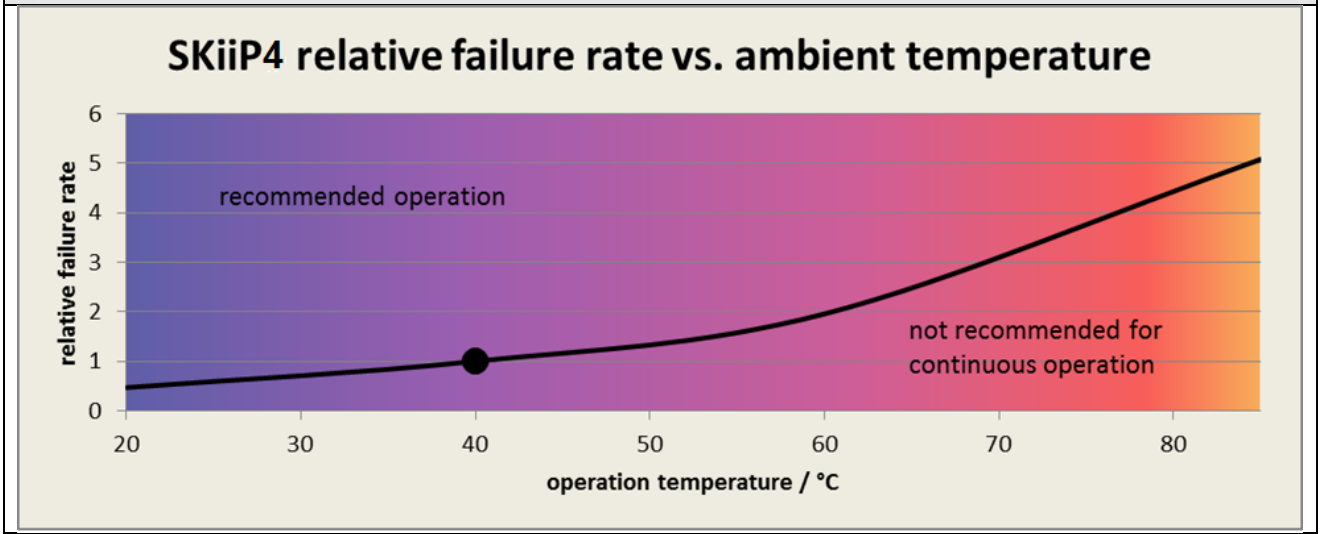
The failure rate describes the probability of a failure within a certain time. Usually, the failure rate follows the so-called bathtub curve, shown in Figure 7.10: high in the beginning (failures known as early failures), then dropping to a low and more or less constant value (the random failures) before it rises again as wear-out begins to set in and end-of-life failures set a limit to the useful life of a component.

Figure 7.10: Probability of a failure during operation time.



The evaluation of the failure rate for different temperatures shows that its expected failure rate roughly doubles for a 20 C increase in operating temperature (see Figure 7.11).

Figure 7.11: SKiiP driver failure rate temperature dependence calculated according to SN29500



The less stress a device is subjected to, the less likely it is to fail. Low operation time, low current, low temperature and low dc-link voltage prolong its life and reduce the failure rate. Therefore, the design has to find a working compromise between exhausting a device to maximum capacity and obtaining an acceptable failure rate and life time.
The following temperature rating is recommended for the SKiiP4 systems:

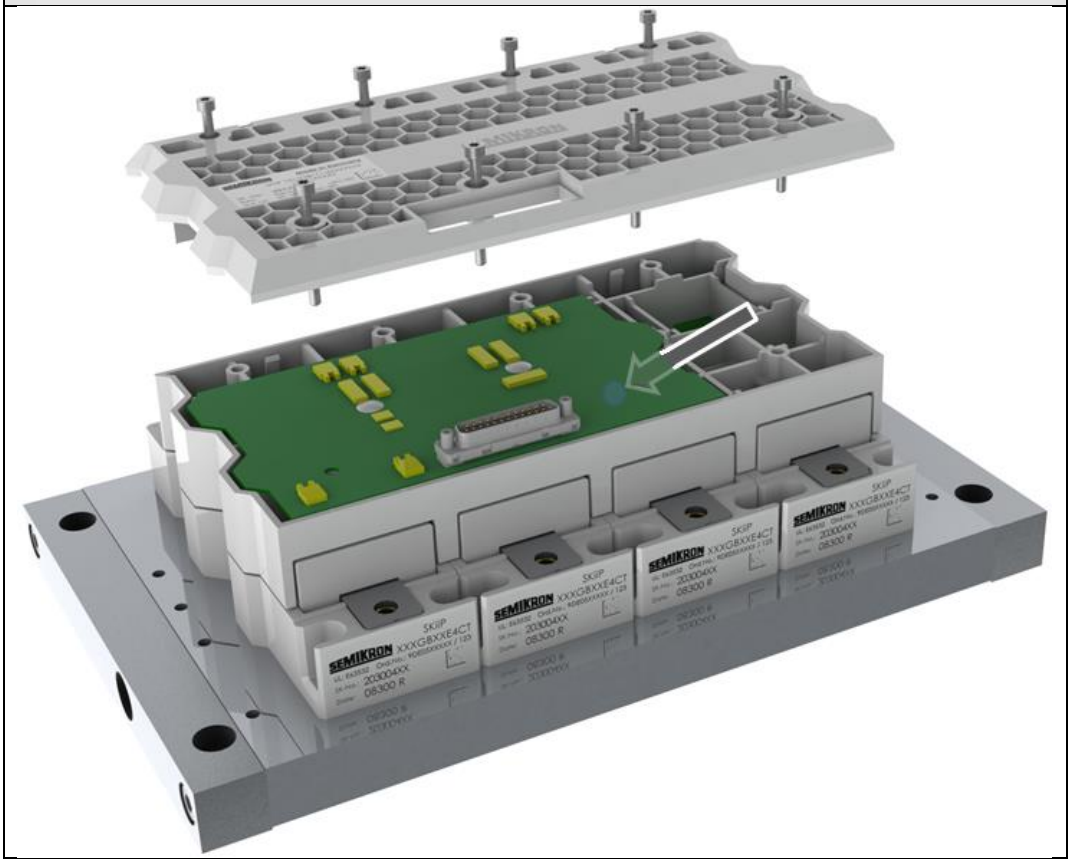
1. Power section: It is necessary to make sure by calculations and measurements that the recommended IGBT and diode junction temperatures are not exceeded also considering overload conditions. The recommended maximum junction temperatures are 150°C which is 25°C lower than the maximum temperature of 175°C. That is to ensure the reliable operation. Calculations can be carried out by the SEMIKRON simulation tool SEMISEL which is available on the SEMIKRON homepage www.semikron.com. Load cycles and cooling conditions can be adapted to meet the application conditions. Measurement of the DCB-sensor temperature (available on the driver connector as analogue voltage signal) has to be carried out to check that the system works as calculated.
2. Gate driver: Although it is fit for operation at T_a = 85°C, it is recommended that the average ambient temperature for the driver board does not exceed 40°C for extended periods of time. For achieving the lower driver temperature the additional air forced cooling for the driver might be necessary. The current T_{driver} in the application could be measured by means of temperature sensor situated on the bottom side of the driver PCB (see Figure 7.12). The value of the sensor could be read out via CAN-bus interface (please refer to the CAN documentation for the further information). If the temperature will exceed the $T_{Driver\ Trip}$ that is given in the SKiiP®4 data sheet the switching will be blocked and an error signal will be indicated. The default values for the $T_{Driver\ Trip}$ are given in the Table 7-3.

Table 7-3: Default values for the $T_{Driver\ Trip}$

	Min. Value	Typ. Value	Max. Value
$T_{Driver\ Trip}$	113	120	124

If necessary the Trip level of the temperature sensor can be adjusted to the lower level via CAN-bus interface.

Figure 7.12: Position of the driver temperature sensor SKiiP4



7.10 Paralleling of SKiiP®4

For parallel operation the following features are necessary to realize:

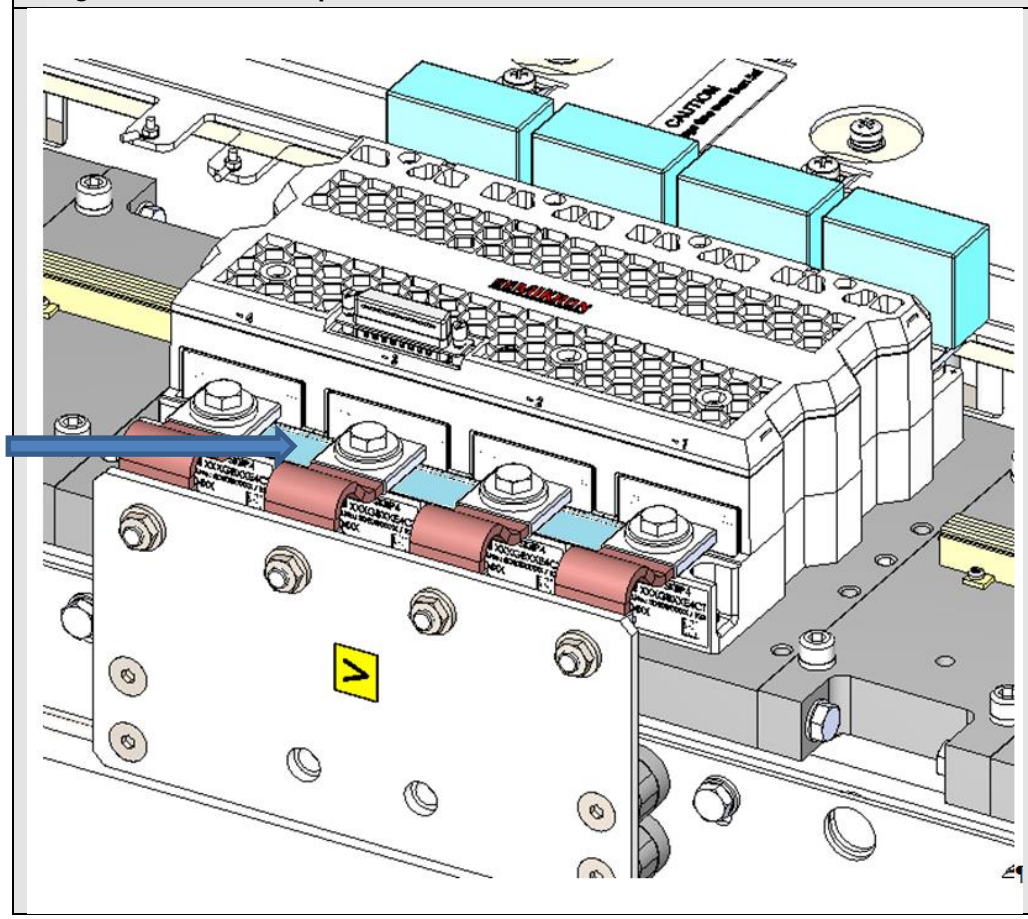
- Common error management for all paralleled SKiiP®4 → Can be realized using the HALT signal
- Monitoring of analog signals, e.g. temperature or current
- one power supply should be used for all subsystems

By using paralleled SKiiPs it has to be made sure that no SKiiP will be overloaded. To ensure this inhomogeneous current has to be limited. This inhomogeneous current is caused by different output voltages of the paralleled inverters which could be a consequence of:

- different propagation time of driver boards
- different switching times of power semiconductors
- tolerance of forward voltage drop of IGBT or diodes
- different DC link voltage levels
- different cooling conditions of paralleled half bridges (e.g. in air cooled applications with thermal stacking)
- different external impedance

The low inductive parallel connection of the AC-terminals can be achieved by an additional flexible **cross connector** directly mounted on the SKiiP AC terminals (marked with an arrow in the Figure 7.13). Please note that the current rating of this bar must not be very high, because there is no load current flowing in this bar. There are only high frequency currents flowing. Thus the flexibility can be achieved by using a comparatively thin material.

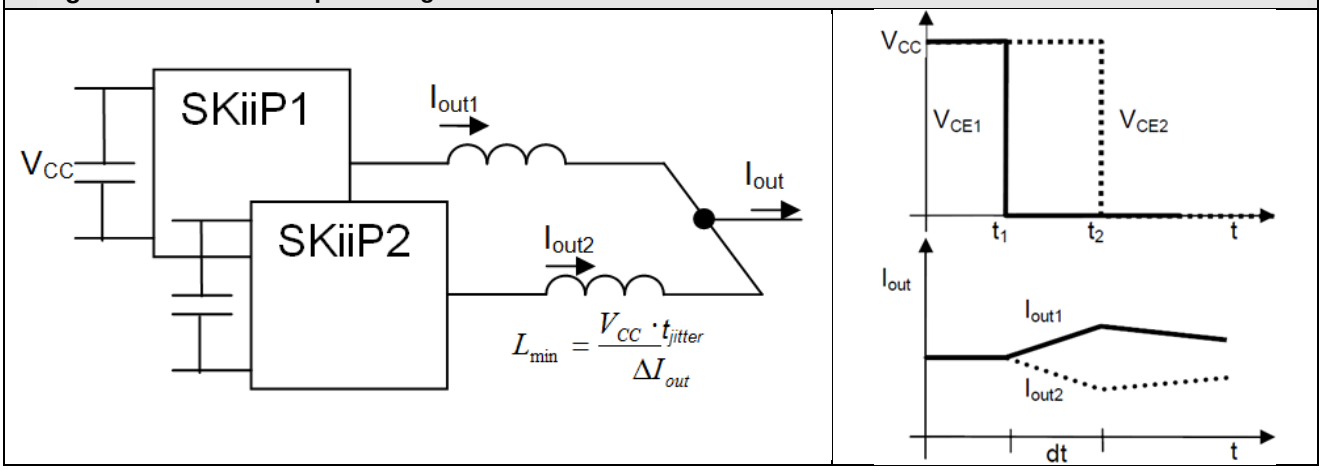
Figure 7.13: An example of SKiiP®4 cross connection



To minimize the above mentioned effects the system designer has to make sure, that there is sufficient inductance between the AC output terminals of the paralleled SKiiP subsystems. The impedance has two tasks:

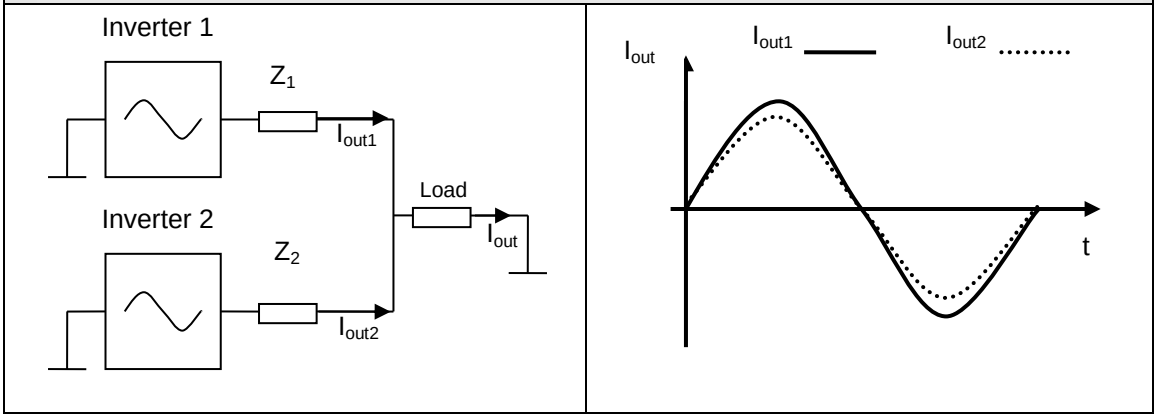
- On the one hand it should prevent the divergence of the current during the switching moment. That could lead to different switching losses, respectively to oscillations. This is shown in Figure 7.14. The value t_{jitter} is given in the SKiiP®4 data sheet on page 2.

Figure 7.14: Effects of paralleling SKiiP®4



- On the other hand a different root mean square value of the output current should be avoided. Symmetric effects come from the inductivities (AC choke) and the ohmic resistors (choke resistor, wiring resistor and path resistance) as shown in Figure 7.15.

Figure 7.15: Schematic Circuit Diagram



Tolerance of forward voltage drop of IGBT or diodes
The IGBTs used in the SKiiPs have a positive temperature coefficient. The free wheeling diodes are produced with a small forward voltage range. Both limit the inhomogeneous current distribution. No further selection of forward voltage groups is necessary.
Different DC link voltage levels
To avoid different output voltages caused by different DC link voltages levels, the DC link should be connected in parallel. It has to be avoided that oscillations between the capacitor banks occur. For large systems fuses between the capacitor banks are recommended. The paralleled systems should have the same DC link with the same capacitor type and capacitor values.
Different cooling conditions of paralleled half bridges
The cooling system of the paralleled SKiiP units should be designed in way to avoid thermal stacking.
In spite of all the mentioned actions it has to be taken into account that for in-homogenous current sharing a de-rating of the nominal current of the power section has to be considered.

7.11 Prevention of condensation

Condensation during operation must be prevented. This can be ensured by regulation of the air or water flow so that the heat sink temperature is always above the environmental temperature. The use of chilled coolant is therefore not recommended. Condensation may also occur because of night/day temperature change. If the power electronic equipment was exposed to humidity or moisture during transport and storage, it should be dried before commissioning. This can be done by air heater in air cooled systems or by pre-heated water in water cooled systems.
.

8 Logistics

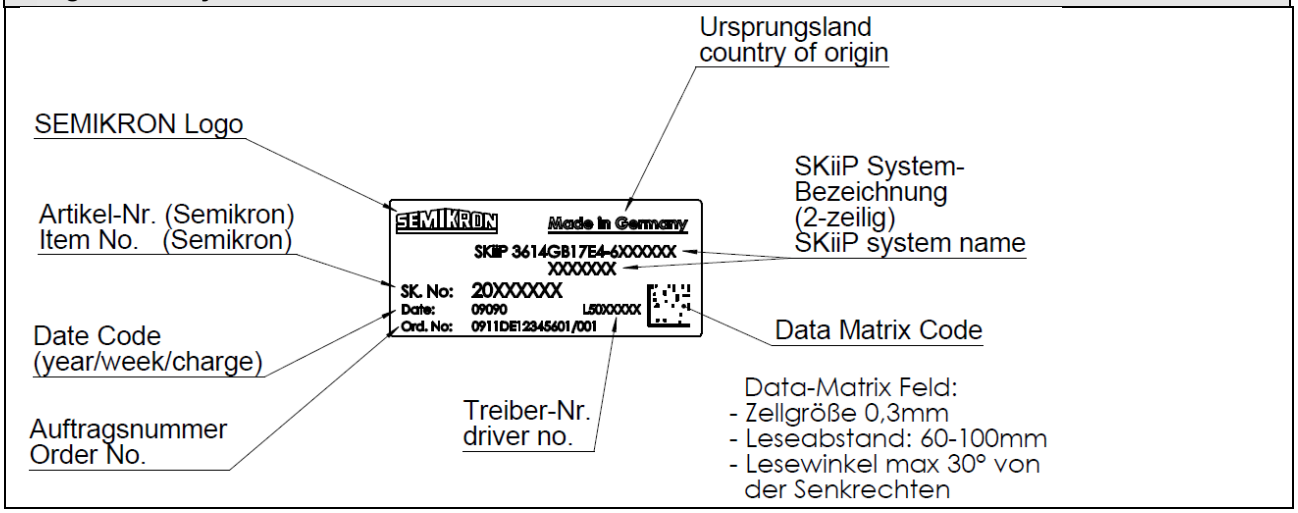
8.1 Label

For reasons of traceability all SKiiP®4 modules are marked with a system, half bridge, driver shuttle and a warranty label.

8.1.1 System Label

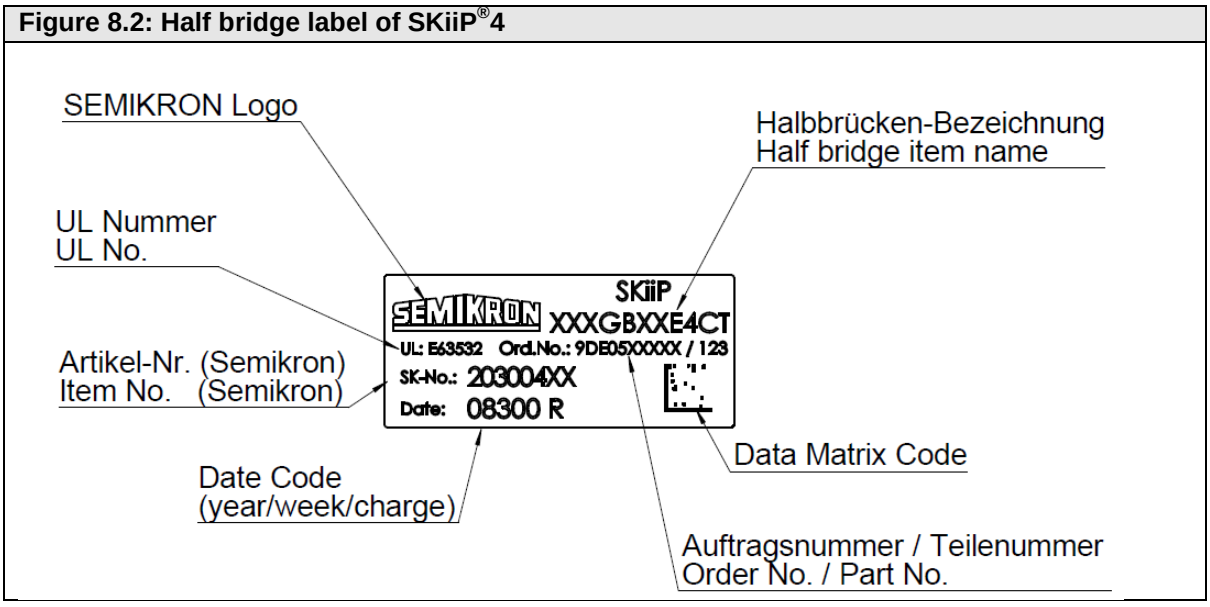
The system label of SKiiP (Figure 8.1) is the label which contains all information necessary for customers. In case of technical inquiries please always name the SKiiP Item number written on this label.

Figure 8.1: System Label of SKiiP®4



8.1.2 Half bridge Laser Label

Figure 8.2: Half bridge label of SKiiP®4



8.1.3 Warranty Label

The warranty label is presented in the Figure 8.3. The position of the warranty label could be found in the corresponding data sheet.

Figure 8.3**: Warranty Label of SKiiP®4**

Please note: Removing the warranty label will result in loss of warranty in case of product reclamation

8.1.4 Data Matrix Code

The Data Matrix Code is described as follows

⇒ Cell size: 0,3mm

⇒ Read distance: 60 – 100mm

⇒ Max. angle of 30° (vertical reference line) for reading

Figure 8.4**:** Data Matrix Code of SKiiP®4

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9 Abbreviations

Abbreviation	Meaning
CTE	Coefficient of Thermal Expansion
DBC	Direct bonded copper
D-Sub	D-Subminiature
EMC	Electromagnetic compatibility
GB	halfbridge configuration
GND	Ground
IGBT	Insulated Gate Bipolar Transistor
IPM	Intelligent Power Module
PCB	Printed Circuit Board
PTC	Positive Temperature Coefficent
RH	Relative Humidity
RoHS	Restriction of Hazardous Substances
SCP	Short Circuit Protection
SKiiP	Semikron intelligent integrated Power
SPS	Short Pulse Suppression
UVP	Under Voltage Protection
SOA	Safe Operating Area

10 Symbols

Symbol	Meaning
I_{Cnom}	Nominal collector current of IGBT
I_{Fnom}	Nominal forward current of diode
$I_{digiout}$	Digital output sink current (HALT-signal)
Q_{PD}	Charge of the Partial Discharge event
$R_{CC´+EE´}$	Resistance of the interconnections between terminals and die
R_{th}	Thermal resistance
$t_{pReset(OCP)}$	Overcurrent reset time
t_{jitter}	Jitter clock time
t_{SIS}	Short pulse suppression time
t_{bl}	Blanking time
t_{POR}	Power-On Reset time
T_a	Ambient temperature
T_j	Junction temperature
T_r	Temperature at reference position
U_{LE}	Line to earth voltage
U_{LL}	Line to line voltage
V_{CEstat}	Collector-Emitter Threshold Static Monitoring Voltage
$V_{it+\ HALT}$	Input threshold voltage HALT-signal (HIGH)
$V_{it-\ HALT}$	Input threshold voltage HALT-signal (LOW)
$T_{DriverTrip}$	Over temperature trip level
$f0_{Uana}$	Bandwidth of DC-voltage measurement @ V_{Dctrip}
$f0_{Iana}$	Bandwidth of current measurement @ I_{TRIPSC}
$f0_{Tana}$	Bandwidth of temperature measurement @ T_{trip}

Symbols and Terms

Letter Symbol	Term
I_{Cnom}	Nominal collector current of IGBT
I_{Fnom}	Nominal forward current of diode
$I_{digiout}$	Digital output sink current (HALT-signal)
Q_{PD}	Charge of the Partial Discharge event
$R_{CC'+EE'}$	Resistance of the interconnections between terminals and die
R_{th}	Thermal resistance
$t_{pReset(OCP)}$	Overcurrent reset time
t_{jitter}	Jitter clock time
t_{SIS}	Short pulse suppression time
t_{bl}	Blanking time
t_{POR}	Power-On Reset time
T_a	Ambient temperature
T_j	Junction temperature
T_r	Temperature at reference position
U_{LE}	Line to earth voltage
U_{LL}	Line to line voltage
V_{Cestat}	Collector-Emitter Threshold Static Monitoring Voltage
$V_{it+ HALT}$	Input threshold voltage HALT-signal (HIGH)
$V_{it- HALT}$	Input threshold voltage HALT-signal (LOW)
$T_{DriverTrip}$	Over temperature trip level
$f0_{Uana}$	Bandwidth of DC-voltage measurement @ V_{Dctrip}
$f0_{Iana}$	Bandwidth of current measurement @ I_{TRIPSC}
$f0_{Tana}$	Bandwidth of temperature measurement @ T_{trip}

A detailled explanation of the terms and symbols can be found in the “Application Manual Power Semiconductors” [2]

References

[1] www.SEMIKRON.com
[2] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, “Application Manual Power Semiconductors”, ISLE Verlag 2011, ISBN 978-3-938843-666